KLI-2113

2098 x 3 Tri-Linear CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 4
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FIGURES

1.1 Features

- **Improved** Tri-linear Color Array
- High Resolution: 2098 pixels
- Wide Dynamic Range
- High Sensitivity
- High Operating Speed
- High Charge Transfer Efficiency
- No Image Lag
- Electronic Exposure Control
- Pixel Summing Capability
- Up to 2.0V peak-peak Output
- 5.0V Clock Inputs
- Two-Phase Register Clocking
- On-chip Dark Reference

1.2 Description

The KLI-2113 is a high resolution, linear array designed for color scanning applications. Each device contains 3 rows of 2098 active photoelements, consisting of high performance 'pinned diodes' for improved sensitivity, lower noise and the elimination of lag. Each row is selectively covered with an improved red, green or blue integral filter stripe for spectral separation. The pixel height and pitch is 14 µm and the center-to-center spacing between color channels is 112 µm, giving an effective eight line delay between adjacent channels during imaging. Readout of the pixel data for each channel is accomplished through the use of a single CCD shift register allowing for a single output per channel with no multiplexing artifacts. Twelve light shielded photoelements are supplied at the beginning of each channel to act as a dark reference. The devices are manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies. The die size is 31.15 mm X 1.73 mm and the chip is housed in a 28-pin, 0.600" wide, dual in-line package. Cover glass is multi-layer AR coated on both sides.

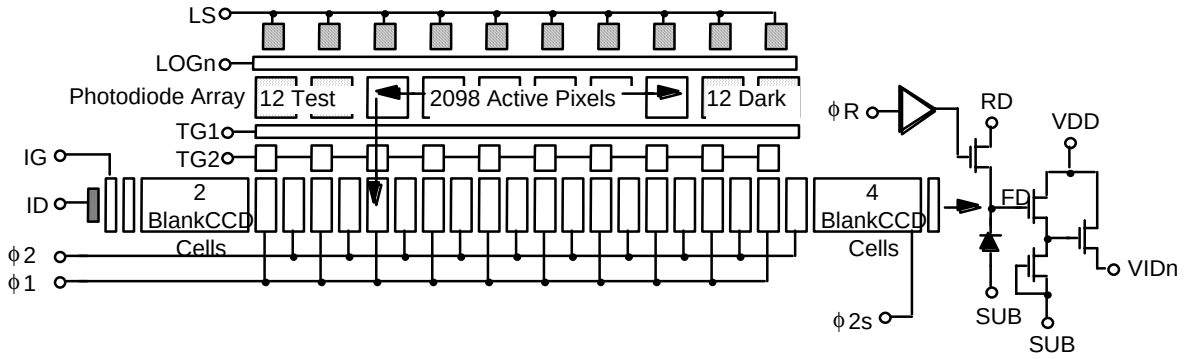


Figure 1 - Single Channel Schematic

1.3 Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the ϕ1 and ϕ2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photo-diode into the TG1 storage region. As TG1 is turned back 'off', charge is transferred through TG2 and into the ϕ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

1.4 Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the 'pinning level' of the photodiode. (The 'pinning' level is the maximum channel potential that the photodiode can achieve

and is fixed by the doping levels of the structure.) With TG1 in an 'off' state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to the timing diagrams, one notes that the exposure can be controlled by pulsing the LOG gate to a 'high' level while TG1 is turning 'off' and then returning the LOG gate to a 'low' bias level sometime during the line scan. The effective exposure (texp) is net time between the falling edge of the LOG gate and the falling edge of the TG1 gate (end of the line). Separate LOG connections for each channel are provided enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably, during the TG1 falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the ϕ1/ϕ2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

1.5 Charge Transport and Sensing

Readout of the signal charge is accomplished by two-phase, complementary clocking of the ϕ1 and ϕ2 gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (4.75V_{p-p} min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the ϕ2 clock. Resettable floating diffusions are used for the charge to voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta V_{FD} = \Delta Q/C_{FD}$. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR.

1.6 Pixel Summing

The effective resolution of this sensor can be varied by enabling the pixel summing feature. A separate pin is provided for the last shift register gate labeled ϕ2s. This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1049 pixels), by supplying a ϕ2s clock which is a 75% duty cycle signal at 1/2 the frequency of the ϕ2 signal, and modifying the ϕR clock as depicted in the timing diagram section. Applications that require full resolution mode (2098 pixels), must tie the ϕ2s pin to the ϕ2 pin. Refer to the timing diagram section for additional details.

1.7 Package Configuration

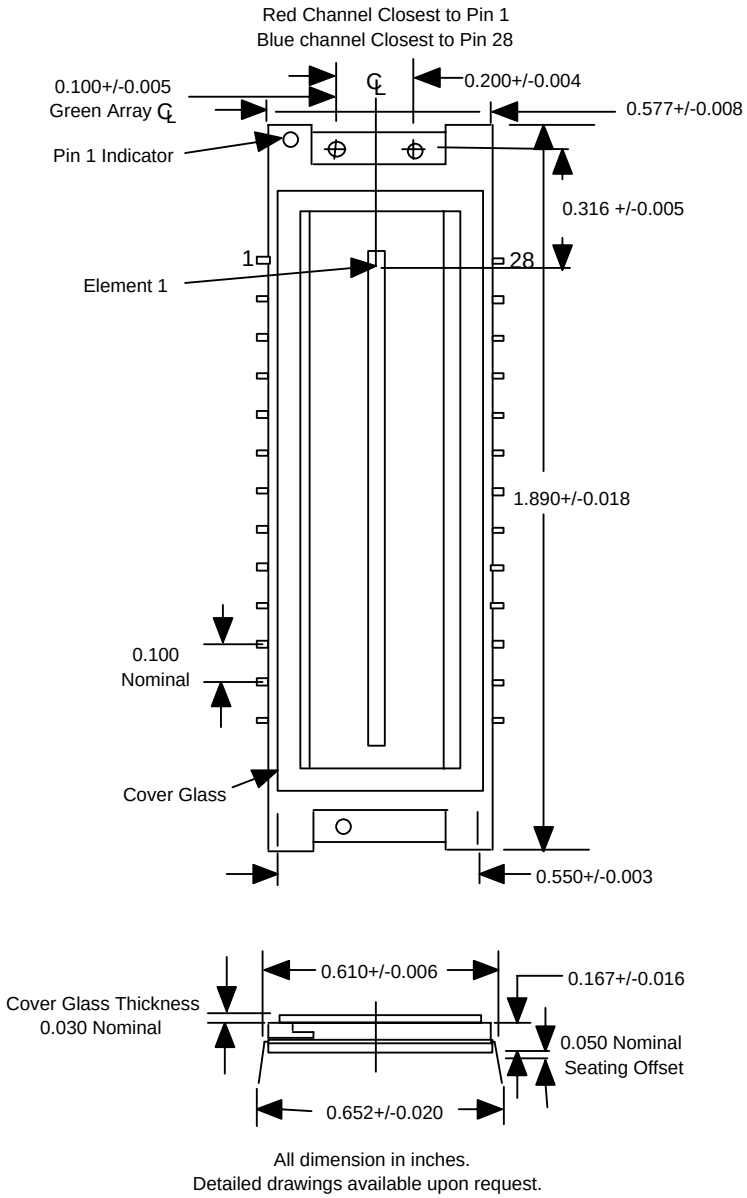


Figure 2 - Packaging Diagram

2.1 Pin Description

Pin	Symbol	Description
1	VIDR	Red output video
2	SUB	Substrate
3	RD	Reset drain
4	ϕR	Reset clock
5	LOGR	Red overflow gate
6	LOGG	Green overflow gate
7	SUB	Substrate
8	n/c	No connection
9	LS	Light shield/Exposure Drain
10	IG	Input gate/LOG test pin
11	TG2	Outer transfer gate
12	n/c	No connection
13	ϕ2s	Phase 2 shift register summing gate clock
14	ϕ2	Phase 2 shift register clock
15	ϕ1	Phase 1 shift register clock
16	n/c	No connection
17	n/c	No connection
18	TG1	Inner transfer gate
19	ID	Input diode test pin
20	n/c	No connection
21	n/c	No connection
22	LOGB	Blue overflow gate
23	n/c	No connection
24	SUB	Substrate
25	VIDB	Blue output video
26	VDD	Amplifier supply
27	SUB	Substrate
28	VIDG	Green output video

2.2 Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Gate Pin Voltages	V_{GATE}	-0.5	+16	V	1, 2
Pin to Pin Voltage	$V_{PIN-PIN}$		16	V	1, 3
Diode Pin Voltages	V_{DIODE}	-0.5	+16	V	1,4
Output Bias Current	I_{DD}		-10	mA	5
Output Load Capacitance	$C_{VID,LOAD}$		15	pF	
CCD Clocking Frequency	f_C		20	MHz	6
Operating Temperature	T_{OP}	0	70	^oC	7
Storage Temperature	T_{ST}	-25	+80	^oC	8

Notes:
1. Referenced to substrate voltage.
2. Includes pins: ϕ1, ϕ2, ϕ2s, TG1, TG2, ϕR, IG, and LOGn.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, RD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal (2MHz) clocking frequency. VIDn load resistor values may need to be decreased as well to achieve required output bandwidths.
7. Noise performance will degrade with increasing temperatures.
8. Long term storage at these temperatures will accelerate color filter degradation.

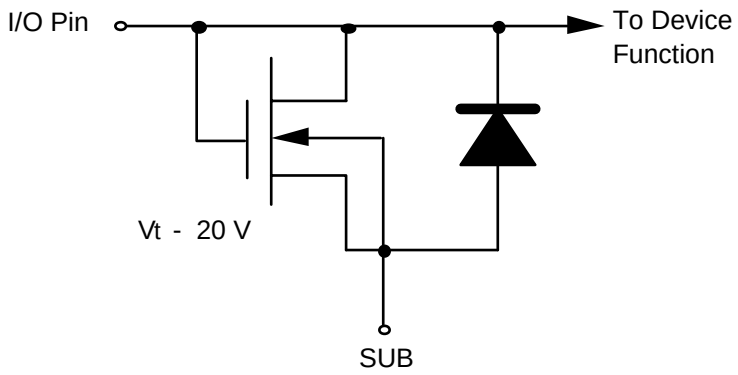


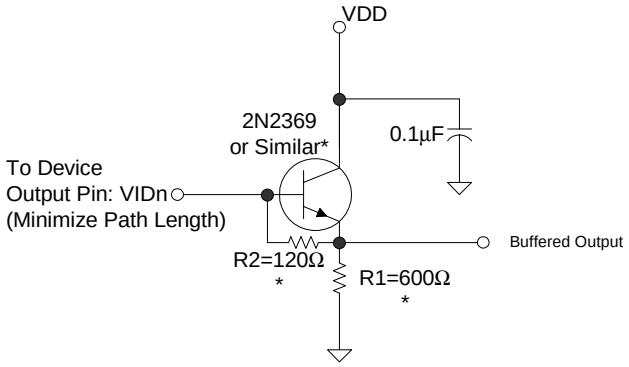
Figure 3 - ESD Protection Circuit

CAUTION: To allow for maximum performance, this device contains limited i/o protection and may be sensitive to electrostatic induced damage. Devices should be installed in accordance with strict ESD handling procedures!

2.3 DC Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{SUB}	Substrate		0		V	
V_{RD}	Reset Drain Bias	+11.5	+12.0	+12.5	V	
V_{DD}	Output Buffer Supply	+11.5	+12.0	+12.5	V	
V_{LS}	Light Shield/Drain Bias	+11.5	+12.0	+12.5	V	
I_{DDn}	Output Bias Current/Ch.	-4.0	-6.0	-8.0	mA	1
V_{IG}	Test Pin-Input Gate/LOG		+12.0		V	
V_{ID}	Test Pin-Input Diode		+12.0		V	

Notes:
1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. See example below.



*Choose values optimized for specific operating frequency. R2 should not be less than 75Ω

Figure 4 - Typical Output Bias/Buffer Circuit

2.4 AC Clock Level Conditions

Symbol	Parameter	Min	Nom.	Max.	Units	Remarks
$V\phi_{1H}$,$V_{\phi 2nH}$	CCD Readout Clocks High	+4.75	+5.0	+5.25	V	
$V\phi_{1L}$,$V_{\phi 2nL}$	CCD Readout Clocks Low	-0.1	0	+0.1	V	
V_{TGnH}	Transfer Clocks High	+4.75	+5.0	+5.25	V	
V_{TGnL}	Transfer Clocks Low	-0.1	0	+0.1	V	
$V_{\phi RH}$	Reset Clock High	+4.75	+5.0	+5.25	V	
$V_{\phi RL}$	Reset Clock Low	-0.1	0	+0.1	V	
V_{LOGnH}	Exposure Clocks High	+4.75	+5.0	+5.25	V	1
V_{LOGnL}	Exposure Clocks Low	-0.1	0	+0.1	V	1

Notes:
1. Tie pin to 0V for applications where exposure control is not used.

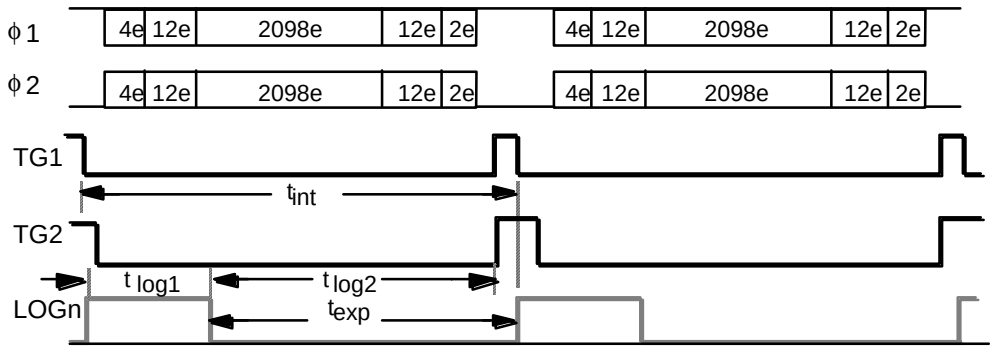
2.5 AC Timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
$1e = 1/f_{CLK}$	CCD Element Duration	50	500		ns	
$1L = t_{int}$	Line/Integration Period	0.108	1.066		ms	
t_{pd}	PD-CCD Transfer Period	1.0			µs	
t_{tg1}	Transfer Gate 1 Clear	500			ns	
t_{tg2}	Transfer Gate 2 Clear	500			ns	
t_{LOG1}	Log Gate Duration	1			µs	
t_{LOG2}	Log Gate Clear	1			µs	
t_{rst}	Reset Pulse Duration	9			ns	
t_{cd}	Clamp to ϕ2 Delay	5			ns	1
t_{sd}	Sample to Reset Edge Delay	5			ns	1
t_r	CCD Clock Rise Time		30		ns	Typical

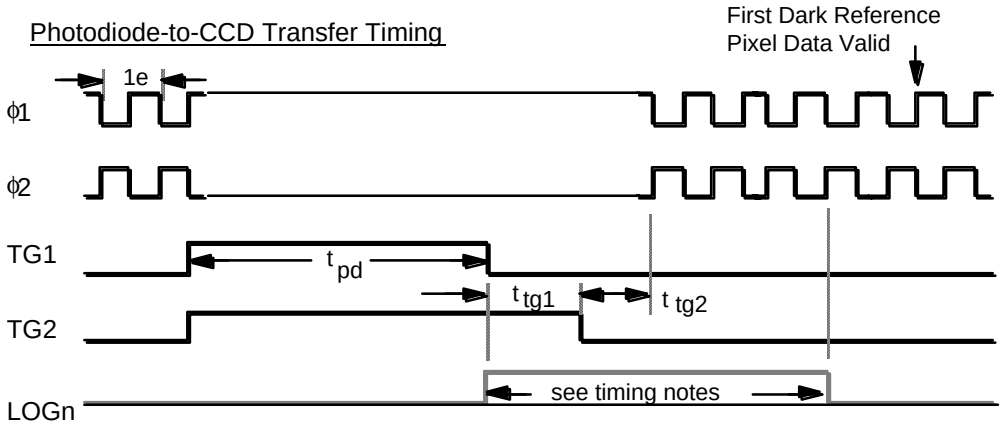
Notes:
1. Recommended delays for correlated double sampling of output.

Timing Diagram

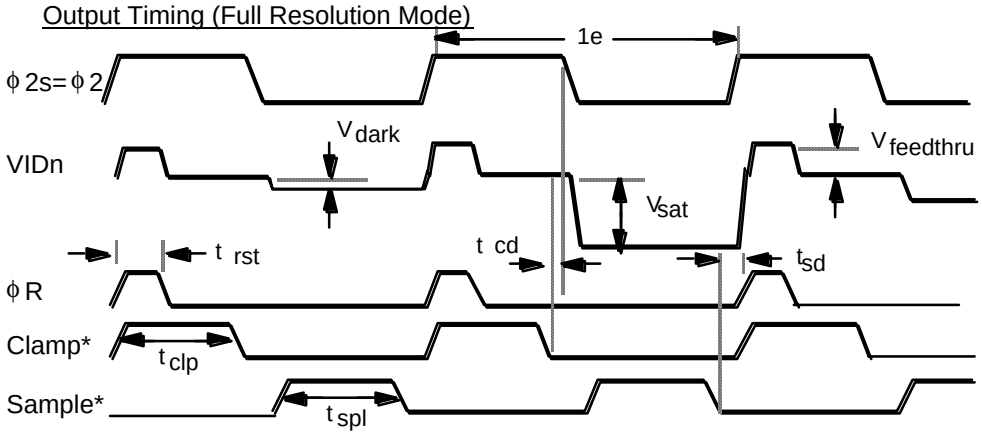
Line Timing



Photodiode-to-CCD Transfer Timing



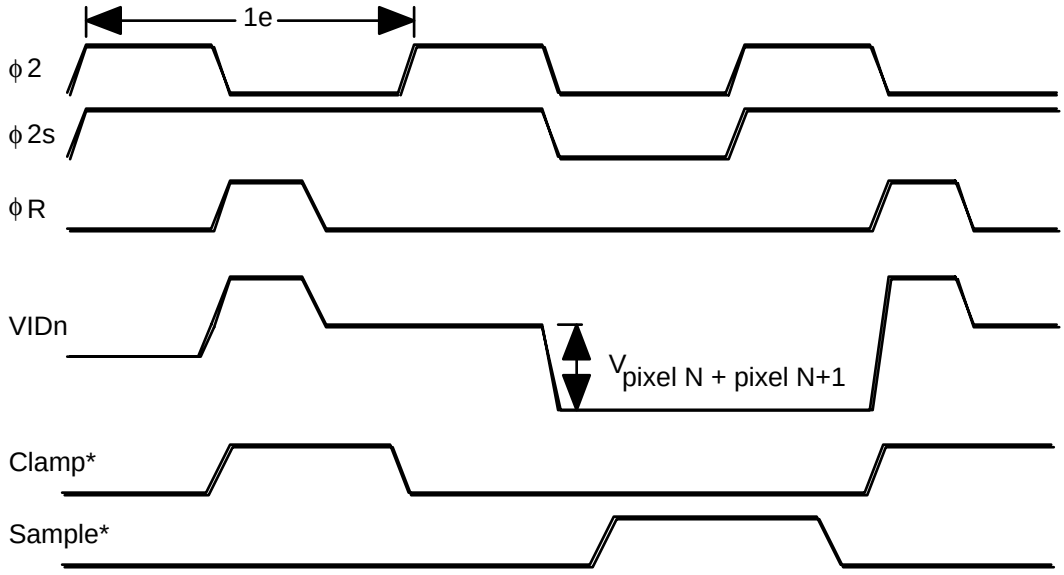
Output Timing (Full Resolution Mode)



* Required for correlated double sampling

Timing Diagram (Continued...)

Output Timing (2-Pixel Summing Mode)



* Required for correlated double sampling

3.1 Image Specifications

Specifications given under nominal operating conditions @ 25°C ambient, f_{CLK} =2 MHz and nominal external VIDn load resistors unless otherwise specified.

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{sat}	Saturation Output Voltage		2.0		V_{p-p}	1, 7
$\Delta V_o/\Delta N_e$	Output Sensitivity		11.5		$\mu V/e^-$	7
$N_{e,sat}$	Saturation Signal Charge		170k		electrons	
R	Responsivity (@ 650nm)		50		$V/\mu J/cm^2$	2, 7
	(@ 540nm)		32		$V/\mu J/cm^2$	
	(@ 460nm)		25		$V/\mu J/cm^2$	
f_{-3dB}	Output Buffer Bandwidth		75		MHz	@ C_{LOAD} = 10 pF
DR	Dynamic Range		76		dB	3
I_{dark}	Dark Current		0.02		pA/pixel	4
CTE, η	Charge Transfer Efficiency		.99999		-	5
L	Lag		0.6	1	%	1st Field
$V_{o,dc}$	DC Output Offset	6	7	9	Volts	7
PRNU	Photoresponse Uniformity		5	10	% p-p	6
C_ϕ	Register Clock Capacitance		500		pF	/phase
C_{TG}	Transfer Gate Capacitance		400		pF	

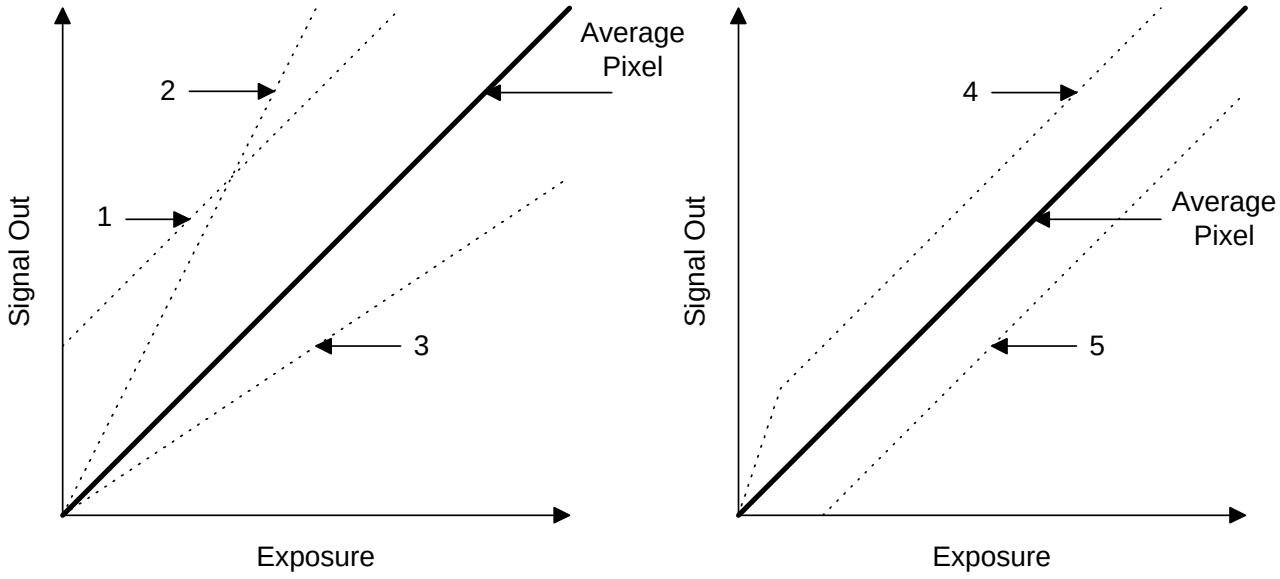
Notes:
1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between ϕ1 and ϕ2 phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +9°C.
5. Measured per transfer. For total line h < $(.99999)^{4256}$ =0.96.
6. Low frequency response across array with color filter array.
7. Decreasing external VIDn load resistors to improve signal bandwidth will decrease these parameters.

3.2 Defect Classification

Test conditions: T=25°C, f_{CLK}=2MHz, t_{int}=1.066msec

Field	Defect Type	Threshold	Units	Notes	Number
Dark	Bright	8.0	mV	1, 2	0
Bright	Bright/Dark	10	%	1, 3	0
Bright	Exposure Control	4.0	mV	1, 4, 5	≤16

Notes:
1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See line 1 in figure below.
3. Pixels whose response is greater or less than the average response by the specified threshold. See lines 2 and 3 in figure below.
4. Pixels whose response deviates from the average pixel response by the specified threshold when operating in exposure control mode. See lines 4 and 5 in the figure below.
5. Defect coordinates are available upon request.



4.1 Quality Assurance and Reliability

4.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

4.1.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

4.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

4.1.4 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe work stations.

4.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions, and can be supplied upon request.

4.1.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

4.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-mail: imagers@kodak.com
Web: www.kodak.com/go/imagers

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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Image Sensor Solutions, Eastman Kodak Company products are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company.

Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

(2 MHz Operation, Emitter Follower Buffered, 3/4 Vsat, Dark to Bright Transition)

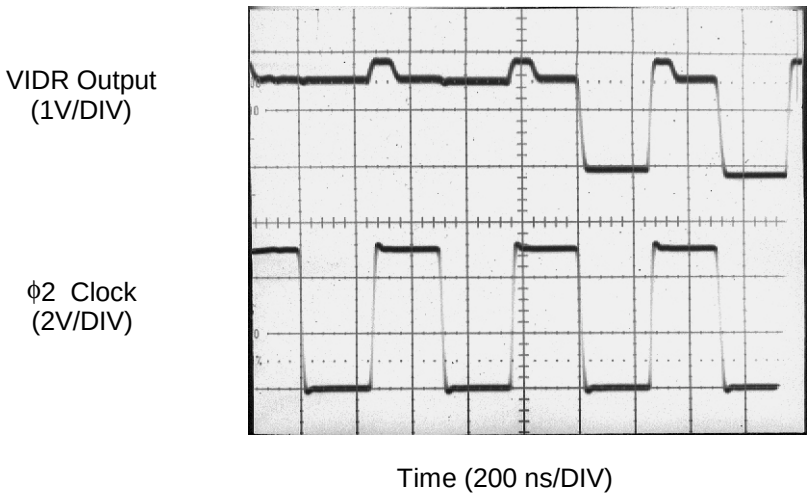
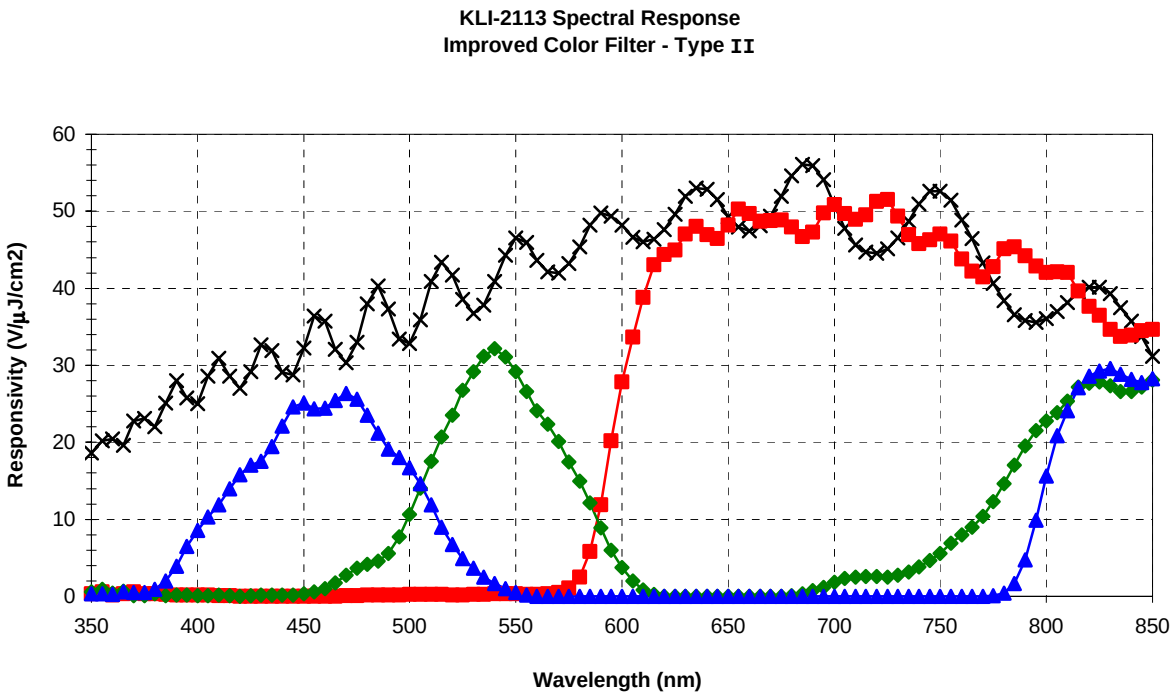


Figure 5 - Output Waveforms



Note: Color filter arrays become transparent after 700nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF.

Figure 6 - Typical Responsivity

Revision Changes:

Revision Number	Changes
4	New Color Filter materials implemented.