DEVICE PERFORMANCE SPECIFICATION

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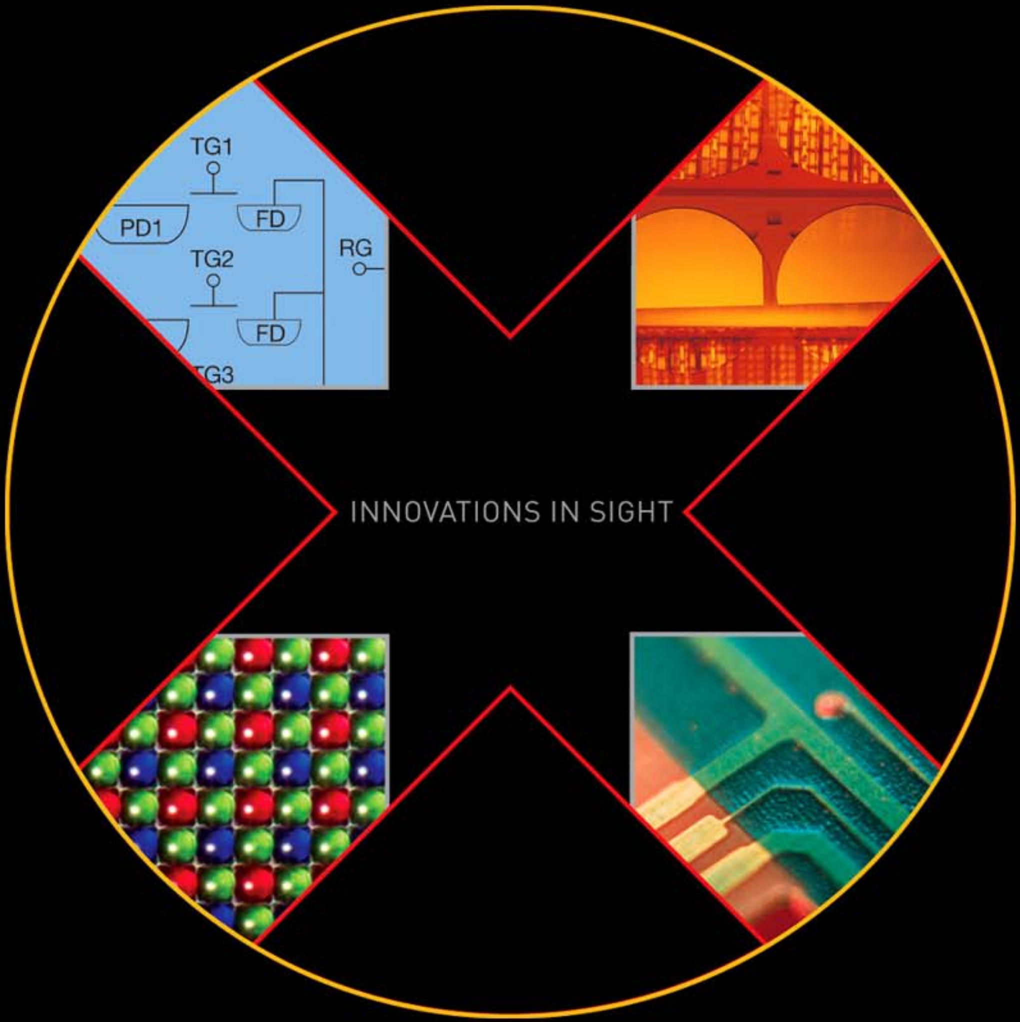

INNOVATIONS IN SIGHT

KODAK KAI-0340 IMAGE SENSOR

640(H) X 480(V) INTERLINE CCD IMAGE SENSOR

Kodak
Image Sensor Solutions

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SUMMARY SPECIFICATION

KODAK KAI-0340 IMAGE SENSOR

640 (H) X 480 (V) INTERLINE TRANSFER PROGRESSIVE SCAN CCD

DESCRIPTION

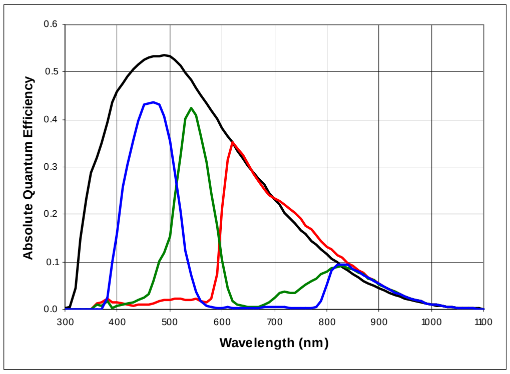
The KODAK KAI-0340 image sensor is a 640 (H) x 480 (V) resolution, 1/3" optical format, progressive scan interline CCD. This image sensor is offered in 2 versions: the KAI-0340-Dual and the KAI-0340-Single. The KAI-0340-Dual will support 210 full resolution frame-per-second readout while the KAI-0340-Single will support 110 frame-per-second readout. Frame rates as high as 2,000 Hz (KAI-0340-Single) and 3,400 Hz (KAI-0340-Dual) can be achieved using the Fast Horizontal Line Dump feature to eliminate horizontal lines during readout and special clocking mode enabled by this sensor. Designed for demanding imaging applications, this sensor has additional features including electronic shuttering, peak QE (quantum efficiency) of 55%, extremely low noise and low dark current. These features give this sensor exceptional sensitivity and make it ideal for machine vision, scientific, surveillance, and other computer input applications. Both sensor versions can also be supplied with Kodak's RGB Bayer color filter array, making it a color sensor for your critical color applications.

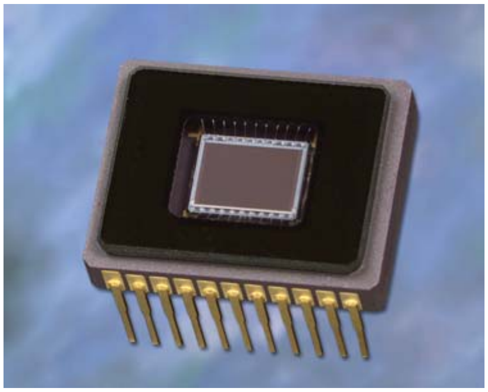
FEATURES

- High sensitivity
- High dynamic range
- Low noise architecture
- High frame rate
- Electronic shutter

APPLICATIONS

- Industrial inspection





Parameter	Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	696 (H) x 492 (V)
Number of Effective Pixels	648 (H) x 484 (V)
Number of Active Pixels	640 (H) x 480 (V)
Pixel Size	7.4 µm (H) x 7.4 µm (V)
Active Image Size	4.736mm (H) x 3.552mm (V) 5.920mm (diagonal) 1/3" optical format
Aspect Ratio	4:3
Number of Outputs	1 or 2
Charge Capacity	40 MHz – 20,000 electrons 20 MHz – 40,000 electrons
Output Sensitivity	30 µV/e
Photometric Sensitivity KAI-0340-ABB	3.61 V/lux-sec
Photometric Sensitivity KAI-0340-CBA	1.17(B), 1.54(G), 0.65(R) V/lux-sec
Readout Noise	40 MHz – 16 electrons 20 MHz – 14 electrons
Dynamic Range	40 MHz – 62 dB 20 MHz – 69 dB
Dark Current	Photodiode < 200 eps VCCD < 1000 eps
Maximum Pixel Clock Speed	40MHz
Maximum Frame Rate	KAI-0340-Dual – 210 fps KAI-0340-Single – 110 fps
Package Type	CerDIP
Package Size	0.500" [12.70mm] width 0.625" [15.87mm] length
Package Pins	22
Package Pin Spacing	0.050"

All parameters above are specified at T = 40°C

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0655	KAI-0340-AAA-CP-AA-Single	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade, Single Output	KAI-0340S
4H0656	KAI-0340-AAA-CP-AE-Single	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Grade, Single Output	
4H0657	KAI-0340-AAA-CP-AA-Dual	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0340D
4H0658	KAI-0340-AAA-CP-AE-Dual	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Grade, Dual Output	
4H0659	KAI-0340-AAA-CF-AA-Single	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass, no coatings, Standard Grade, Single Output	KAI-0340S
4H0660	KAI-0340-AAA-CF-AE-Single	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass, no coatings, Engineering Grade, Single Output	
4H0661	KAI-0340-AAA-CF-AA-Dual	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0340D
4H0662	KAI-0340-AAA-CF-AE-Dual	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass, no coatings, Engineering Grade, Dual Output	
4H0872	KAI-0340-ABA-CP-AA-Single	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade, Single Output	KAI-0340ABBS
4H0873	KAI-0340-ABA-CP-AE-Single	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Grade, Single Output	
4H0874	KAI-0340-ABA-CP-AA-Dual	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0340ABBD
4H0875	KAI-0340-ABA-CP-AE-Dual	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Grade, Dual Output	
4H0868	KAI-0340-ABA-CB-AA-Single	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Standard Grade, Single Output	KAI-0340ABBS
4H0869	KAI-0340-ABA-CB-AE-Single	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Engineering Grade, Single Output	
4H0870	KAI-0340-ABA-CB-AA-Dual	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0340ABBD
4H0871	KAI-0340-ABA-CB-AE-Dual	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Engineering Grade, Dual Output	
4H0663	KAI-0340-CBA-CB-AA-Single	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Standard Grade, Single Output	KAI-0340SCM
4H0664	KAI-0340-CBA-CB-AE-Single	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Engineering Grade, Single Output	
4H0665	KAI-0340-CBA-CB-AA-Dual	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Standard Grade, Dual Output	KAI-0340DCM
4H0666	KAI-0340-CBA-CB-AE-Dual	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass, no coatings, Engineering Grade, Dual Output	
4H0472	KEK-4H0472-KAI-0340-10-40	Evaluation Board (Complete Kit)	n/a

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

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DEVICE DESCRIPTION

ARCHITECTURE

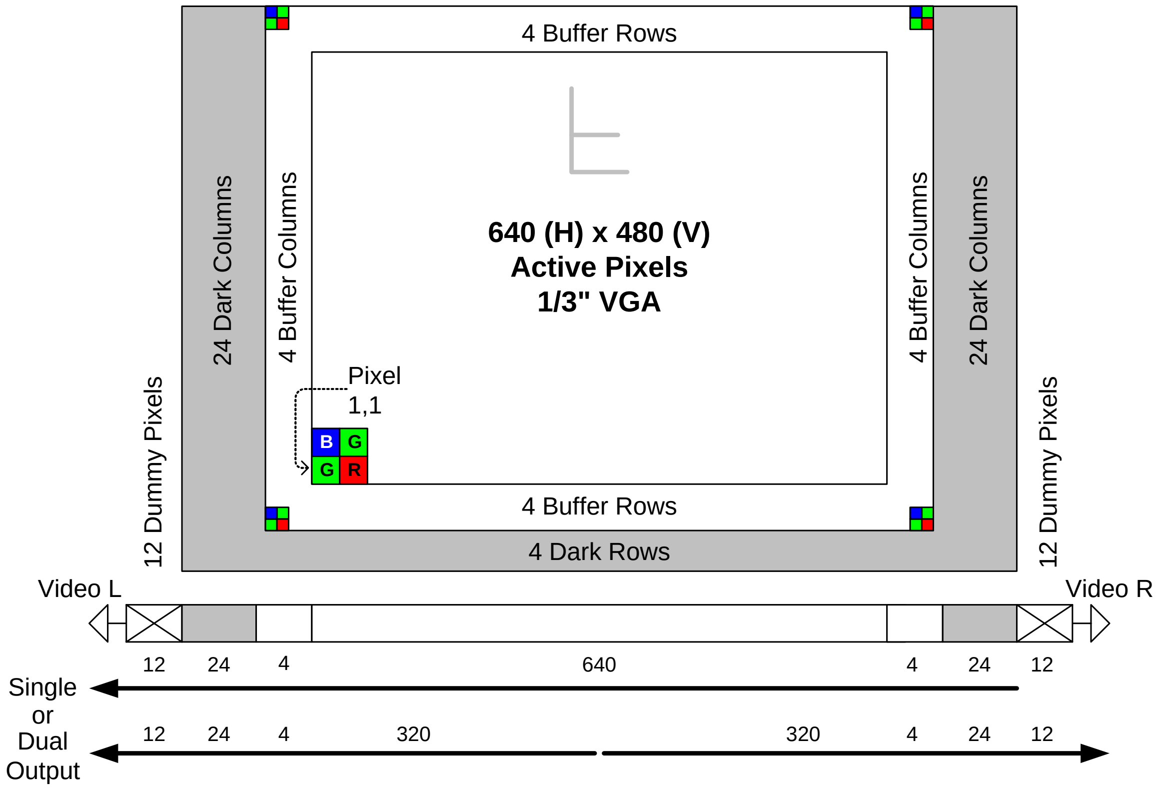


Figure 1: Sensor Architecture

There are 4 light-shielded rows followed by 488 photoactive rows. The first 4 and the last 4 photoactive rows are buffer rows giving a total of 480 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 12 empty pixels of each line do not receive charge from the vertical shift register. The next 24 pixels receive charge from the left light-shielded edge followed by 648 photosensitive pixels and finally 24 more light-shielded pixels from the right edge of the sensor. The first and last 4 photosensitive pixels are buffer pixels giving a total of 640 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 12 empty pixels followed by 24 light-shielded pixels followed by 324 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

There are no dark reference rows at the top and 4 dark rows at the bottom of the image sensor. The 4 dark rows are not entirely dark and so should not be used for a dark reference level. Use the 24 dark columns on the left or right side of the image sensor as a dark reference.

Of the 24 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 22 columns of the 24 column dark reference.

ESD PROTECTION

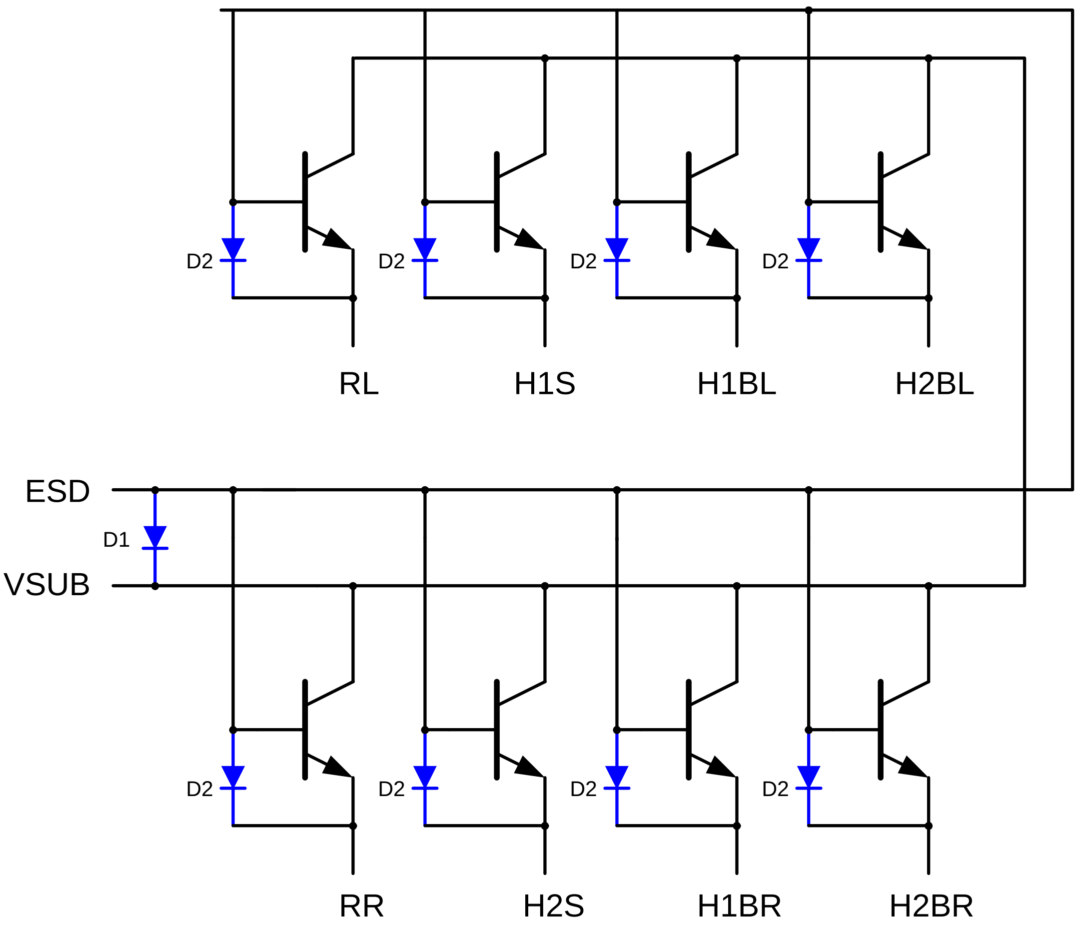


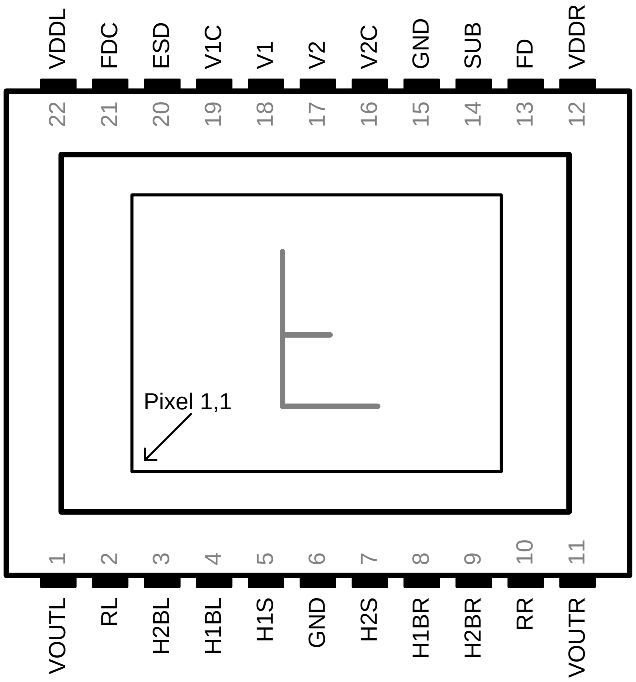
Figure 2: ESD Protection

The ESD protection on the KAI-0340 is implemented using bipolar transistors. The substrate (SUB) forms the common collector of all the ESD protection transistors. The ESD pin is the common base of all the ESD protection transistors. Each protected pin is connected to a separate emitter as shown in Figure 2 - ESD Protection.

The ESD circuit turns on if the base-emitter junction voltage exceeds 17 V. Care must be taken while operating the image sensor, especially during the power on sequence, to not forward bias the base-emitter or base-collector junctions. If it is possible for the camera power up sequence to forward bias these junctions then diodes D1 and D2 should be added to protect the image sensor. Put one diode D1 between the ESD and VSUB pins. Put one diode D2 on each pin that may forward bias the base-emitter junction. The diodes will prevent large currents from flowing through the image sensor. Note that external diodes D1 and D2 are optional and are only needed if it is possible to forward bias any of the junctions.

Note that diodes D1 and D2 are added external to the KAI-0340 CCD.

PIN DESCRIPTION AND PHYSICAL ORIENTATION



Pin	Name	Description
1	VOUTL	Video Output, Left
2	RL	Reset Gate, Left
3	H2BL	Horizontal Clock, Phase 2, Barrier, Left
4	H1BL	Horizontal Clock, Phase 1, Barrier, Right
5	H1S	Horizontal Clock, Phase 1, Storage
6	GND	Ground
7	H2S	Horizontal Clock, Phase 2, Storage
8	H1BR	Horizontal Clock, Phase 1, Barrier, Right
9	H2BR	Horizontal Clock, Phase 2, Barrier, Right
10	RR	Reset Gate, Right
11	VOUTR	Video Output, Right

Pin	Name	Description
22	VDDL	Vdd, Left
21	FDC	Fast Line Dump Gate, Center Columns
20	ESD	ESD
19	V1C	Vertical Clock, Phase 1, Center Rows
18	V1	Vertical Clock, Phase 1, Top and Bottom Rows
17	V2	Vertical Clock, Phase 2, Top and Bottom Rows
16	V2C	Vertical Clock, Phase 2, Center Rows
15	GND	Ground
14	SUB	Substrate
13	FD	Fast Line Dump Gate, Left and Right Columns
12	VDDR	Vdd, Right

Notes:

1. The pins are on a 0.050" spacing
2. If the vertical windowing option is not to be used, then the V1 and V1C pins should be driven from one clock driver. The V2 and V2C pins should also be driven from one clock driver.
3. If the fast dump windowing option is not to be used, then the FD and FDC pins should be driven from the same clock driver.
4. The VOUTR pin is not enabled in the KAI-0340-Single version.

PERFORMANCE

POWER - ESTIMATED

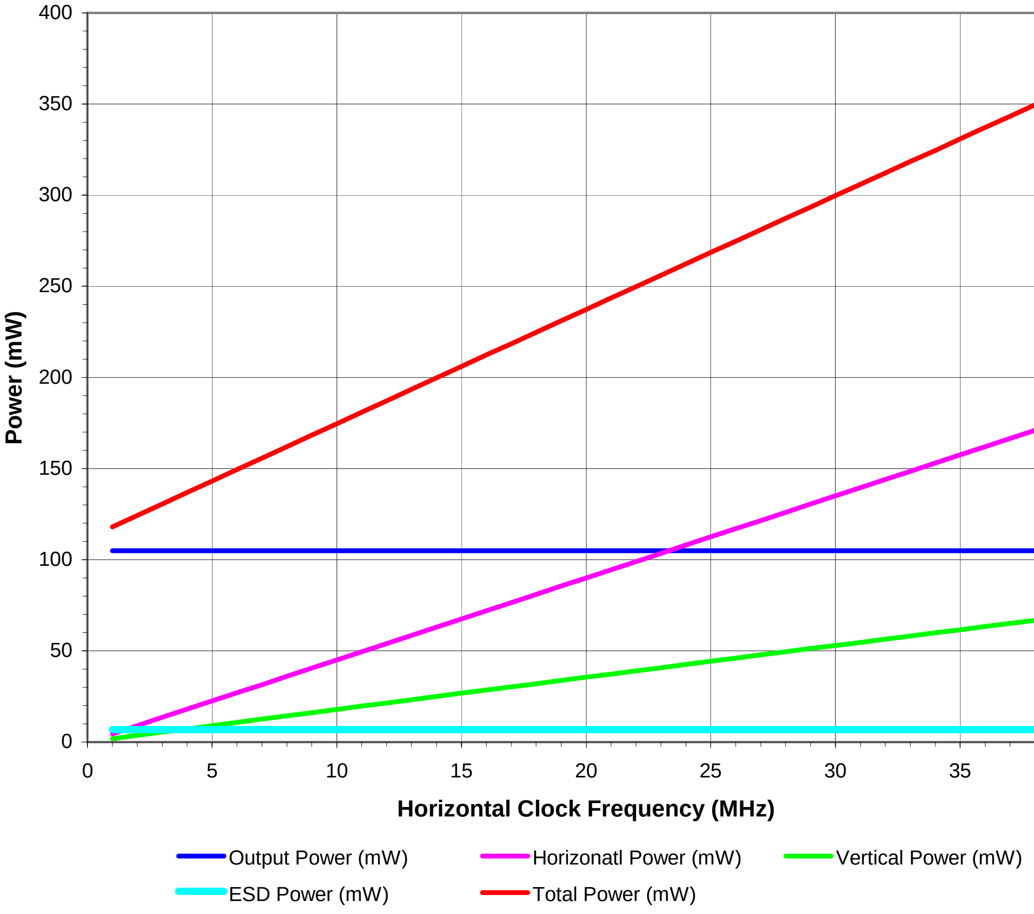


Figure 3: Power

FRAME RATES

Frames rates are for continuous mode operation.

Description	KAI-0340-Single and KAI-0340-Dual Single Output (fps)	KAI-0340-Dual Only Dual Output (fps)
640 x 480	112	214
228 x 480	306	581
640 x 164	325	618
228 x 164	877	1637
228 x 55	2000	3400

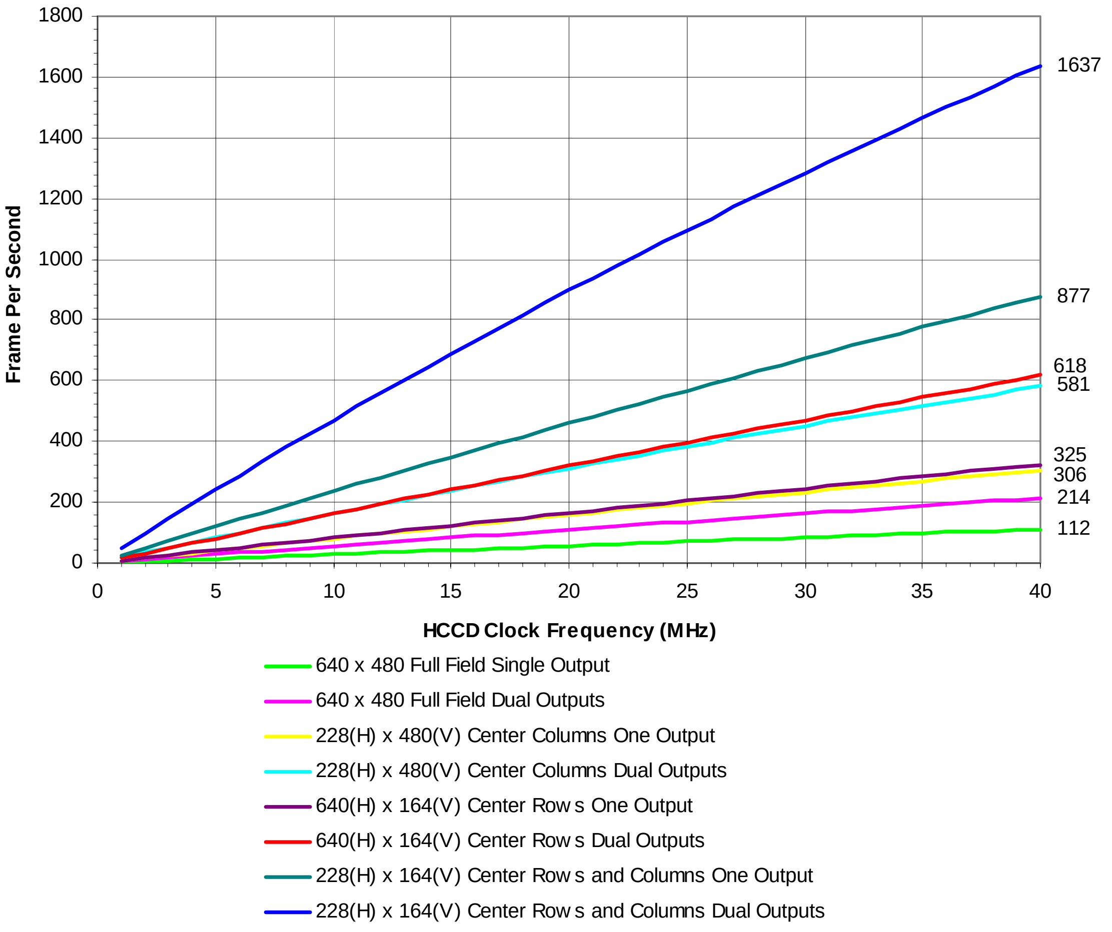


Figure 4: Frame Rates

IMAGING PERFORMANCE

Imaging Performance Operational Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Frame Time	53 msec	1
Horizontal Clock Frequency	10 MHz	
Light Source	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2,3
Operation	Nominal operating voltages and timing	

Notes:

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

Imaging Performance Specifications

All Versions

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Photodiode CCD Dark Current	Ipd	0	40	200	e/p/s	Die	27, 40		
Vertical CCD Dark Current	Ivd	0	400	1000	e/p/s	Die	27, 40		
Dark Current Doubling Temperature		n/a	7	n/a	°C	Design			
Horizontal CCD Charge Capacity	HNe	80	n/a	n/a	ke^-	Design			
Vertical CCD Charge Capacity	VNe	50	n/a	n/a	ke^-	Design			
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	n/a	n/a		Design			
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	n/a	n/a		Design			
Image Lag	Lag	0	<10	50	e^-	Design			
Antiblooming Factor	Xab	100	300	n/a		Design			
Vertical Smear	Smr	n/a	80	75	dB	Design			
Output Amplifier DC Offset	Vodc	6	n/a	12	V	Die		1	
Output Amplifier Impedance	Rout	100	150	200	Ohms	Die		2	
Output Amplifier Bandwidth	F-3db	n/a	140	n/a	MHz	Design			
Output Amplifier Sensitivity	ΔVΔ/N	n/a	30	n/a	µV/e	Design			

Monochrome Versions
with and without microlens

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Global Uniformity		0.0	1.5	3.0	%rms	Die	27, 40		1
Global Peak to Peak Uniformity	PRNU	0.0	5.0	10.0	%pp	Die	27, 40		2
Center Uniformity		0.0	0.6	1.0	%rms	Die	27, 40		3
Photometric Sensitivity KAI-0340M		n/a	3.61	n/a	V/lux-sec	Design		4	

Color Versions
with microlens

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes	Test
Global Uniformity		0.0	2.0	5.0	%rms	Die	27, 40	3	1
Global Peak to Peak Uniformity	PRNU	0.0	5.0	10.0	%pp	Die	27, 40	3	2
Center Uniformity		0.0	1.0	2.0	%rms	Die	27, 40	3	3
Photometric Sensitivity Blue (B) Pixels		n/a	1.17	n/a	V/lux-sec	Design		4	
Photometric Sensitivity Green (G) Pixels		n/a	1.54	n/a	V/lux-sec	Design		4	
Photometric Sensitivity Red (R) Pixels		n/a	0.65	n/a	V/lux-sec	Design		4	

n/a: not applicable

Notes:

1. Measured at sensor output with constant current load of Iout = -5mA and during the floating diffusion reset interval (R high).
2. Last stage only. CLOAD=10pf. Then F-3dB = (1 / (2π*Rout*CLOAD)).
3. Per color.
4. Calculated using quantum efficiency, output amplifier sensitivity, 3200K Plankian source and a CM500S IR-cut filter.

Defect Definitions

Monochrome Versions

Description	Definition	Maximum	Temperature(s) tested at (°C)	Notes	Test
Major dark field defective pixel	Defect >= 16mV	2	27, 40		4
Major bright field defective pixel	Defect >= 11%	0	27, 40		5
Minor dark field defective pixel	Defect >= 4mV	100	27, 40		4
Dead pixel	Defect >= 80%	0	27, 40		5
Saturated pixel	Defect >= 30mV	0	27, 40		4
Cluster defect	A group of 2 to 10 contiguous major defective pixels	0	27, 40		
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	27, 40		

Color Versions

Description	Definition	Maximum	Temperature(s) tested at (°C)	Notes	Test
Major dark field defective pixel	Defect >= 16mV	2	27, 40		4
Major bright field defective pixel	Defect >= 11%	2	27, 40		5
Minor dark field defective pixel	Defect >= 4mV	100	27, 40		4
Dead pixel	Defect >= 80%	0	27, 40		5
Saturated pixel	Defect >= 30mV	0	27, 40		4
Cluster defect	A group of 2 to 10 contiguous major defective pixels	0	27, 40		
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	27, 40		

Defect Map

No defect maps are available for the KAI-0340 image sensor.

Quantum Efficiency

Monochrome with Microlens Quantum Efficiency

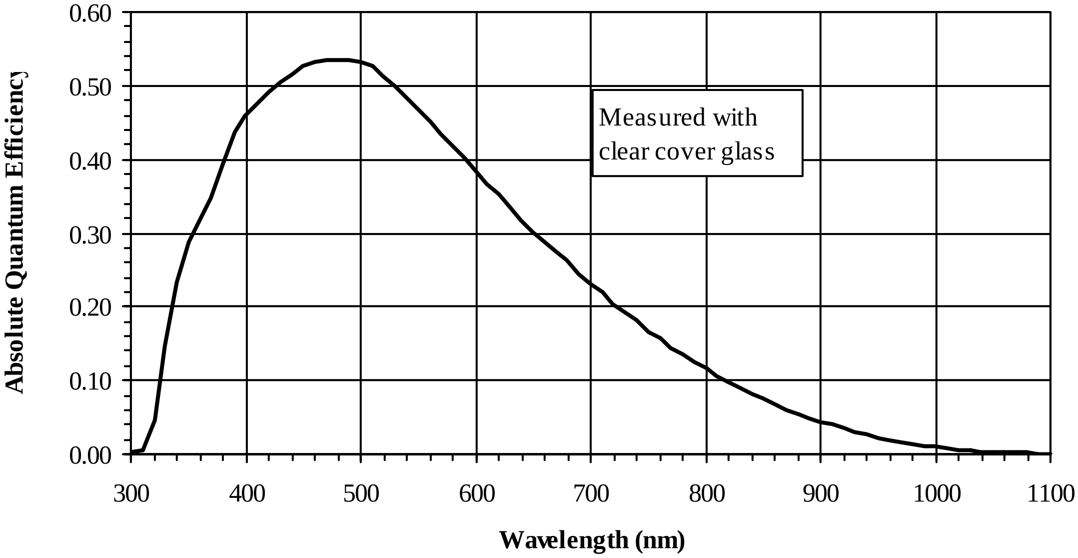


Figure 5: Monochrome with Microlens Quantum Efficiency

Color with Microlens Quantum Efficiency

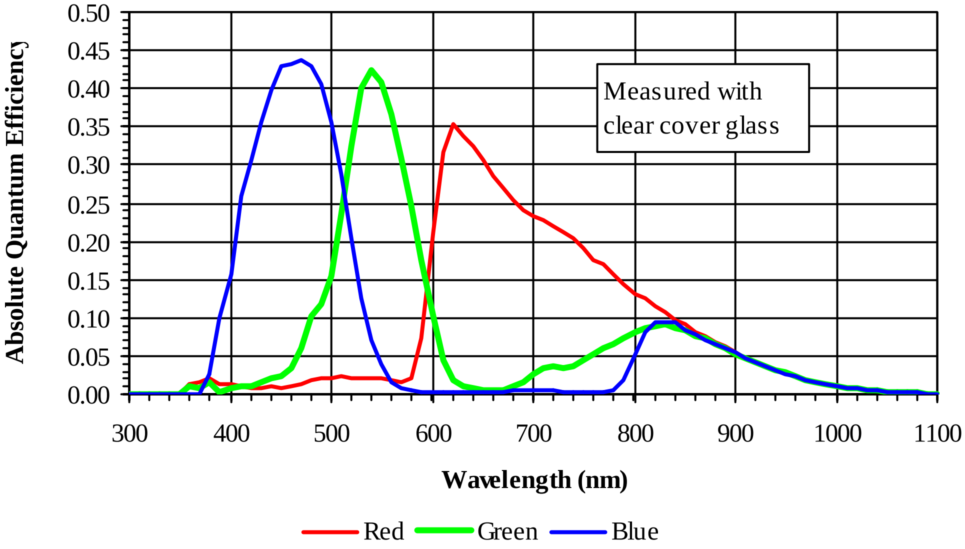


Figure 6: Color with Microlens Quantum Efficiency

Monochrome without Microlens Quantum Efficiency

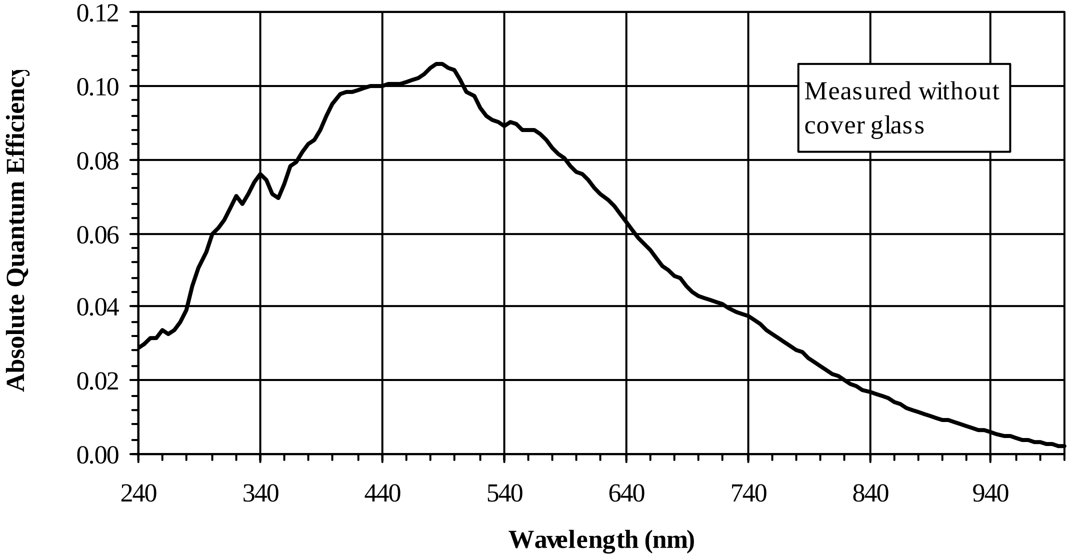


Figure 7: Monochrome without Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

monochrome with microlens

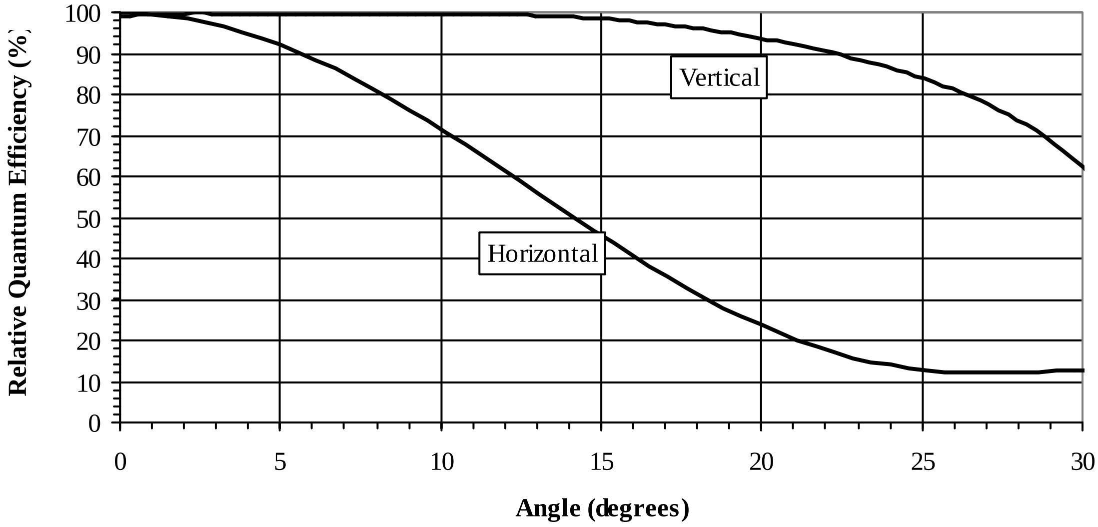


Figure 8: Angular Quantum Efficiency

TEST DEFINITIONS

TEST REGIONS OF INTEREST

Active Area ROI:	Pixel 1, 1 to Pixel 640,480
Center 100 by 100 ROI:	Pixel 270,190 to Pixel 369,289

Only the active pixels are used for performance and defect tests.

TEST SUB REGIONS OF INTEREST

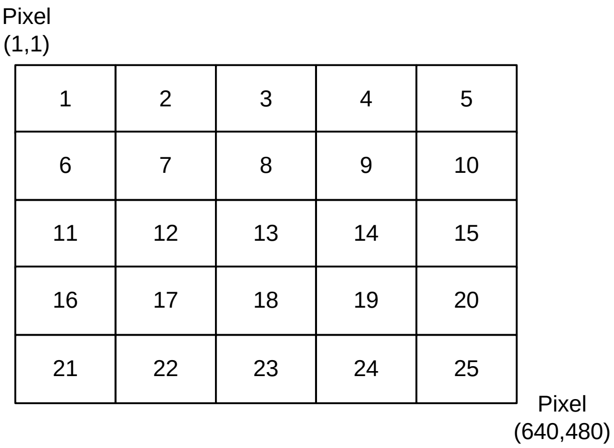


Figure 9: Test Sub Regions of Interest

OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 10 for a pictorial representation of the regions.

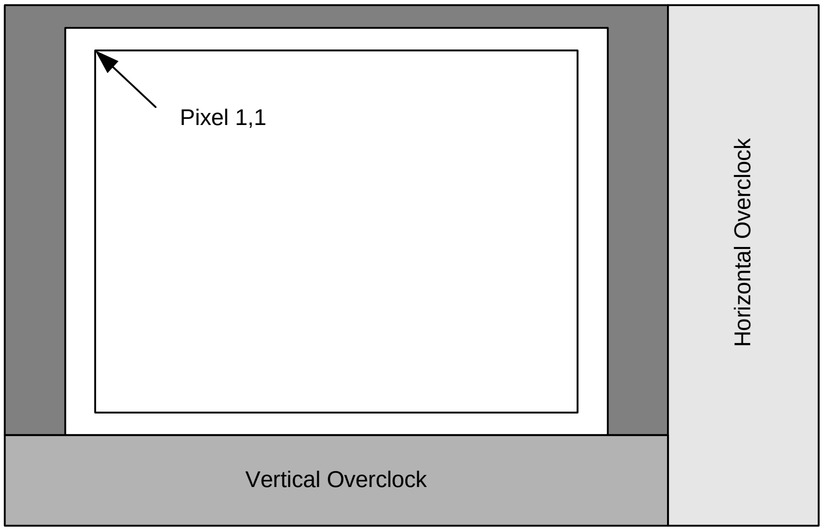


Figure 10: Overclock Regions of Interest

TESTS

1. Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. Global non-uniformity is defined as

$$\text{Global Non-Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right) \quad \text{Units: \%rms}$$

Active Area Signal = Active Area Average – Horizontal Overclock Average

2. Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. The sensor is partitioned into 25 sub regions of interest, each of which is 128 by 96 pixels in size. The average signal level of each of the 25 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

A[i] = (ROI Average – Horizontal Overclock Average)
Where i = 1 to 25. During this calculation on the 25 sub regions of interest, the maximum and minimum average signal levels are found.

The global peak to peak non-uniformity is then calculated as:

$$\text{Global Non-Uniformity} = 100 * \frac{\text{A[i] Maximum Signal - A[i] Minimum Signal}}{\text{Active Area Signal}} \quad \text{Units: \%pp}$$

Active Area Signal = Active Area Average – Horizontal Overclock Average

3. Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Test Regions of Interest) of the sensor. Center non-uniformity is defined as:

$$\text{Center ROI Non-Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right) \quad \text{Units: \%rms}$$

Center ROI Signal = Center ROI Average – Horizontal Overclock Average

4. Dark field defect test

This test is performed under dark field conditions. The sensor is partitioned into 25 sub regions of interest, each of which is 128 by 96 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in “Defect Definitions” section.

5. Bright field defect test

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold
Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 25 sub regions of interest, each of which is 128 by 96 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 420 mV.
- Dark defect threshold: 420mV * 11% = 46 mV
- Bright defect threshold: 420mV * 11% = 46 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 128,96.
  - Median of this region of interest is found to be 420 mV.
  - Any pixel in this region of interest that is >= (420+46 mV) 466 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is <= (420-46 mV) 374 mV in intensity will be marked defective.
- All remaining 24 sub-regions of interest are analyzed for defective pixels in the same manner.

For the color sensor, each color channel is threshold independently.

OPERATION

MAXIMUM RATINGS

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	10	mA	3
Off-chip Load	C_L	n/a	10	pF	4

Notes:

1. Noise performance will degrade at higher temperatures.
2. T=25ºC. Excessive humidity will degrade MTTF.
3. Each output. See Figure 11: Output Amplifier. Note that the current bias affects the amplifier bandwidth.
4. With total output load capacitance of CL = 10pF between the outputs and AC ground.
5. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

MAXIMUM VOLTAGE RATINGS BETWEEN PINS

Description	Minimum	Maximum	Units	Notes
RL, RR, H1S, H2S, H1BL, H2BL, H1BR, H2BR to ESD	0	17	V	
Pin to Pin with ESD Protection	-17	17	V	1
VDDL, VDDR to GND	0	25	V	

Notes:

1. Pins with ESD protection are: RL, RR, H1S, H2S, H1BL, H2BL, H1BR, and H2BR.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Amplifier Supply	VDD	14.75	15.0	15.25	V	2.5 mA	1, 4
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	VAB	15.0	V		2
ESD Protection	ESD	-9.25	-9.0	-8.75	V	2.0 mA	3
Output Bias Current	Iout	0.0	5.0	10.0	mA		5

Notes:

1. The maximum DC current is for one output unloaded and is shown as Ird + Iss in Figure 11. This is the maximum current that the first two stages of one output amplifier plus the reset drain bias circuit will draw. This value is with Vout disconnected.
2. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The shipping container will be marked with two VAB voltages. One VAB will be for a 600mV charge capacity and the other VAB will be for a 1200mV charge capacity. The 600mV charge capacity is for operation of the horizontal clock at frequencies greater than 20 MHz. The 1200mV charge capacity VAB value may be used for horizontal clock frequencies at or below 20MHz.
3. VESD must be more negative than H1L, H2L and RL during sensors operation AND during camera power turn on.
4. Both VDDL and VDDR must both be supplied.
5. One output.

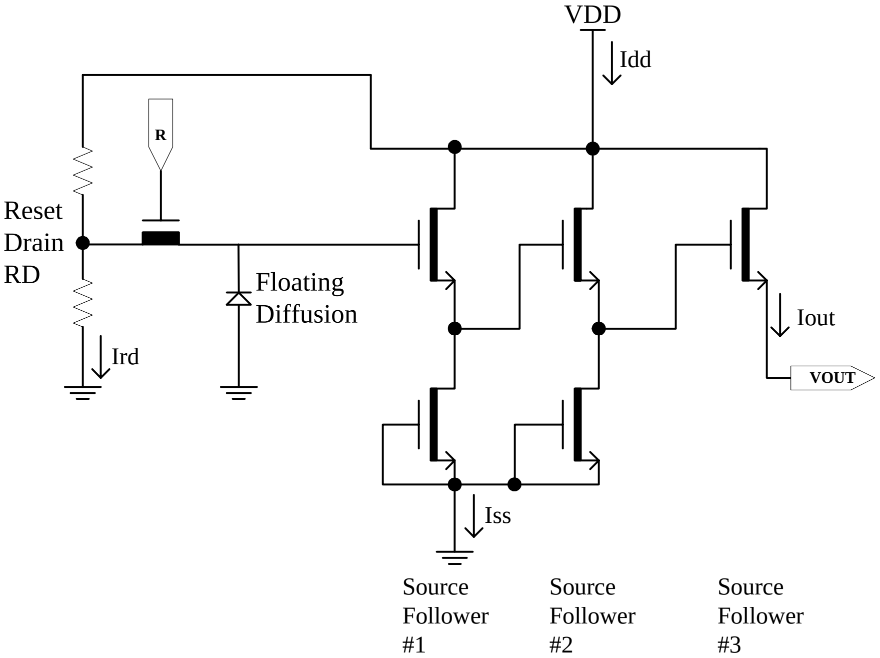


Figure 11: Output Amplifier

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	9.5	+10.0	10.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	-0.2	+0.0	+0.2	V	
Vertical CCD Clocks Low	V1L, V2L	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks High	H1H, H2H	-0.5	+0.0	+0.5	V	1
Horizontal CCD Clocks Low	H1L, H2L	-5.5	-5.0	-4.5	V	1
Reset Clock High	RH	+1.5	+2.0	+2.5	V	2
Reset Clock Low	RL	-3.5	-3.0	-2.5	V	2
Electronic Shutter Voltage	VES	44	48	52	V	
Fast Dump High	FDH	+4.0	+5.0	+5.5	V	
Fast Dump Low	FDL	-9.5	-9.0	-8.5	V	

Notes:

1. The amplitude of the horizontal clock must be at least 4.5 volts.
2. The amplitude of the reset clock must be at least 4.5 volts.

Clock Line Capacitances

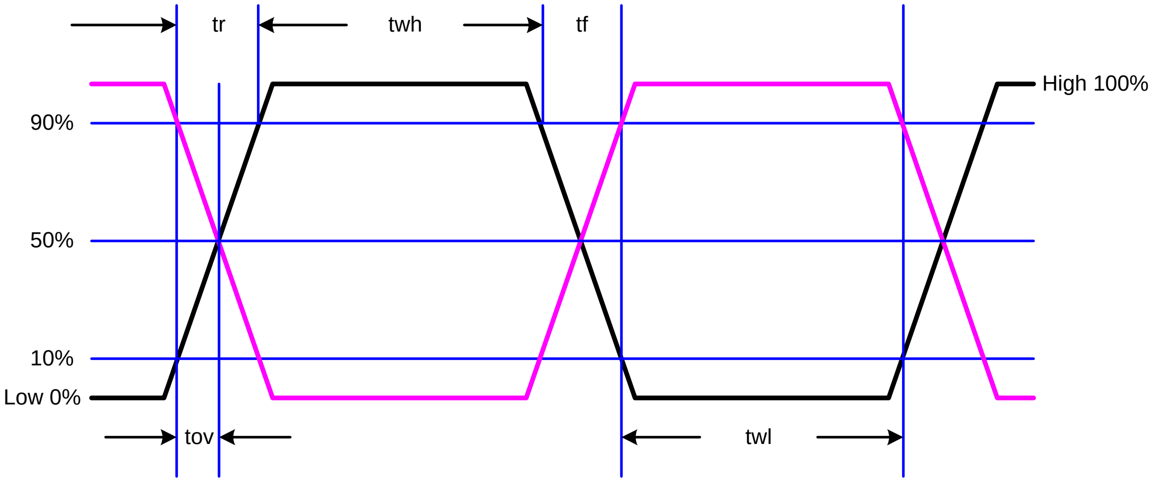
PIN	Approximate Capacitance	Units
V1C	3	nF
V1	5	nF
V2	5	nF
V2C	2	nF
H2BL	25	pF
H1BL	25	pF
H1S	40	pF
H2S	40	pF
H1BR	25	pF
H2BR	25	pF
RL	20	pF
RR	20	pF
FD	30	pF
FDC	25	pF

TIMING REQUIREMENTS

Description	Symbol	Minimum	Units	Notes
HCCD Delay	T_{HD}	200	ns	
VCCD Transfer Time	T_{VCCD}	200	ns	
Photodiode Transfer Time	T_{V3rd}	300	ns	
VCCD Pedestal Time	T_{3P}	15	µs	
VCCD Delay	T_{3D}	5	µs	
VCCD Frame Delay	T_{3L}	15	µs	
VCCD Line End Delay	T_{EL}	25	ns	
HCCD Clock Period	T_H	25	ns	1
Reset Pulse Time	T_R	2.5	ns	
Shutter Pulse Time	T_S	1.0	µs	
Shutter Pulse Delay	T_{SD}	1.0	µs	
Fast Line Dump Delay	T_{FD}	75	ns	

Description	Symbol	Minimum	Units	Notes
VCCD Clock Overlap	T_{OV}	50	%	

Notes:
1. For operation at the minimum HCCD clock period (40MHz), the substrate voltage must be set to limit the signal at the output to 600 mV.
2. Each clock pulse width is defined for twh or twl.



TIMING SEQUENCES

Timing Sequence A

Photodiode to VCCD transfer, entire image.

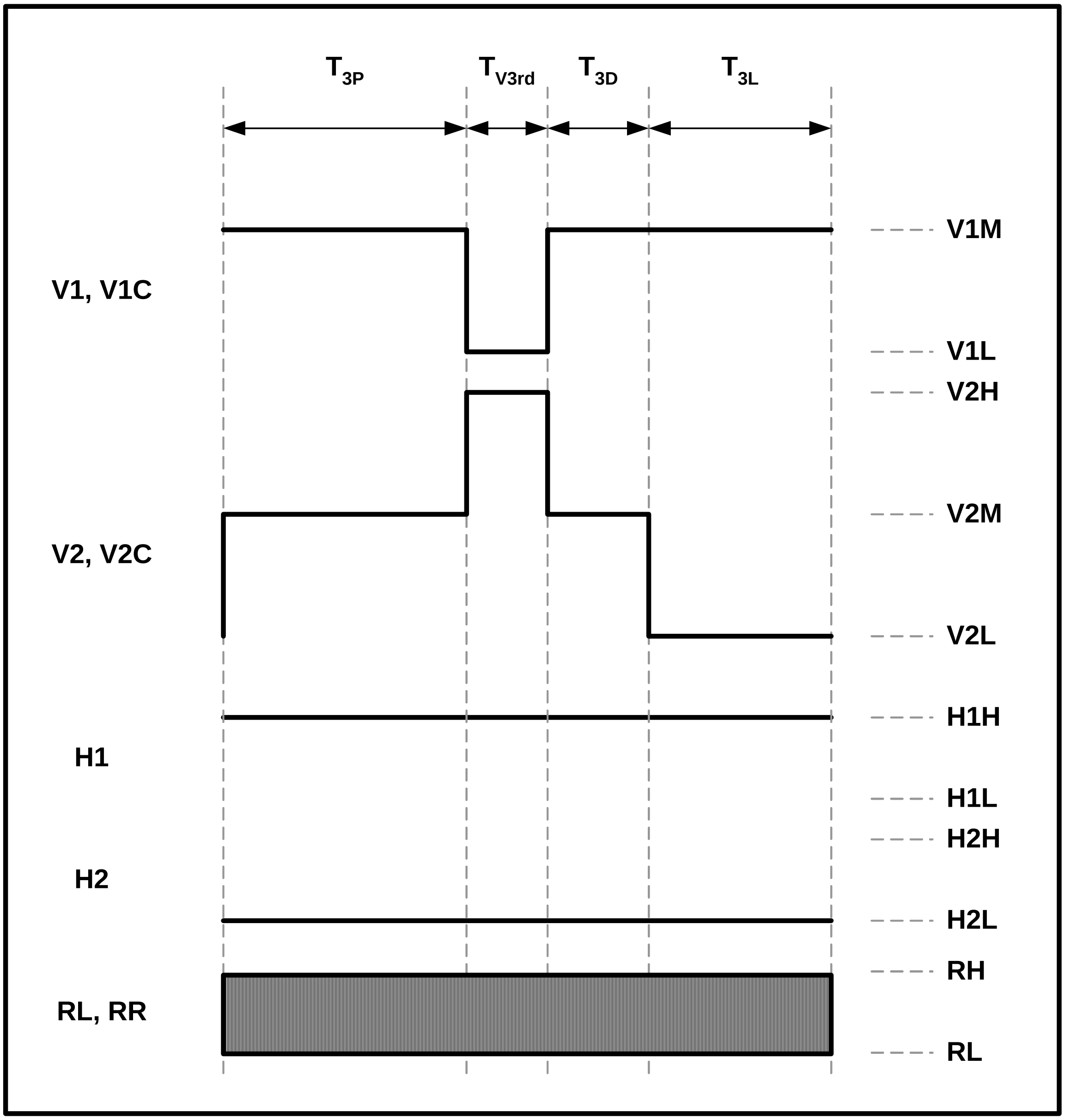


Figure 12: Timing Sequence A

Timing Sequence B

Vertical CCD line shift and horizontal CCD readout of one line.

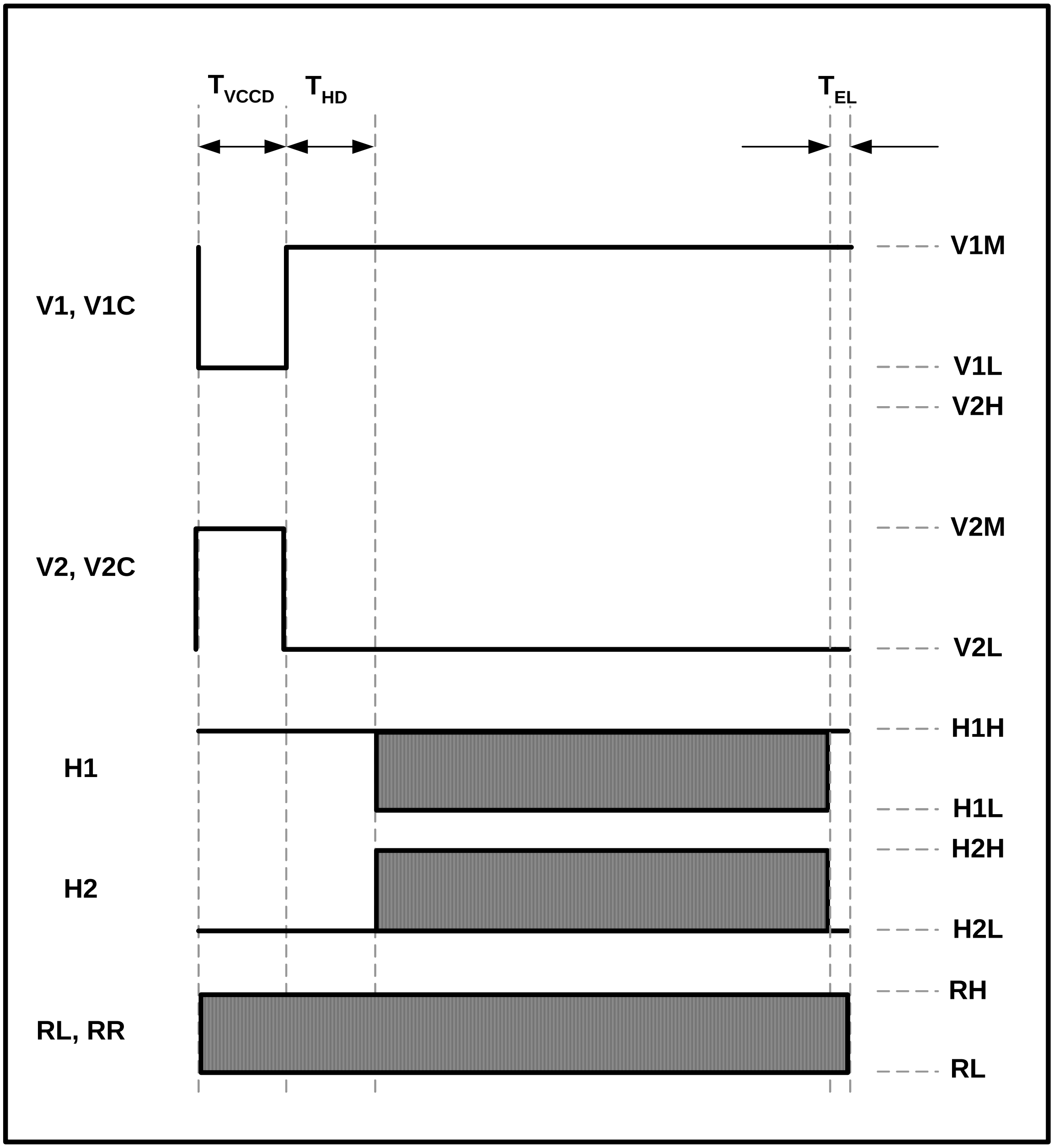


Figure 13: Timing Sequence B

Timing Sequence C

Photodiode to VCCD transfer, center 164 rows.

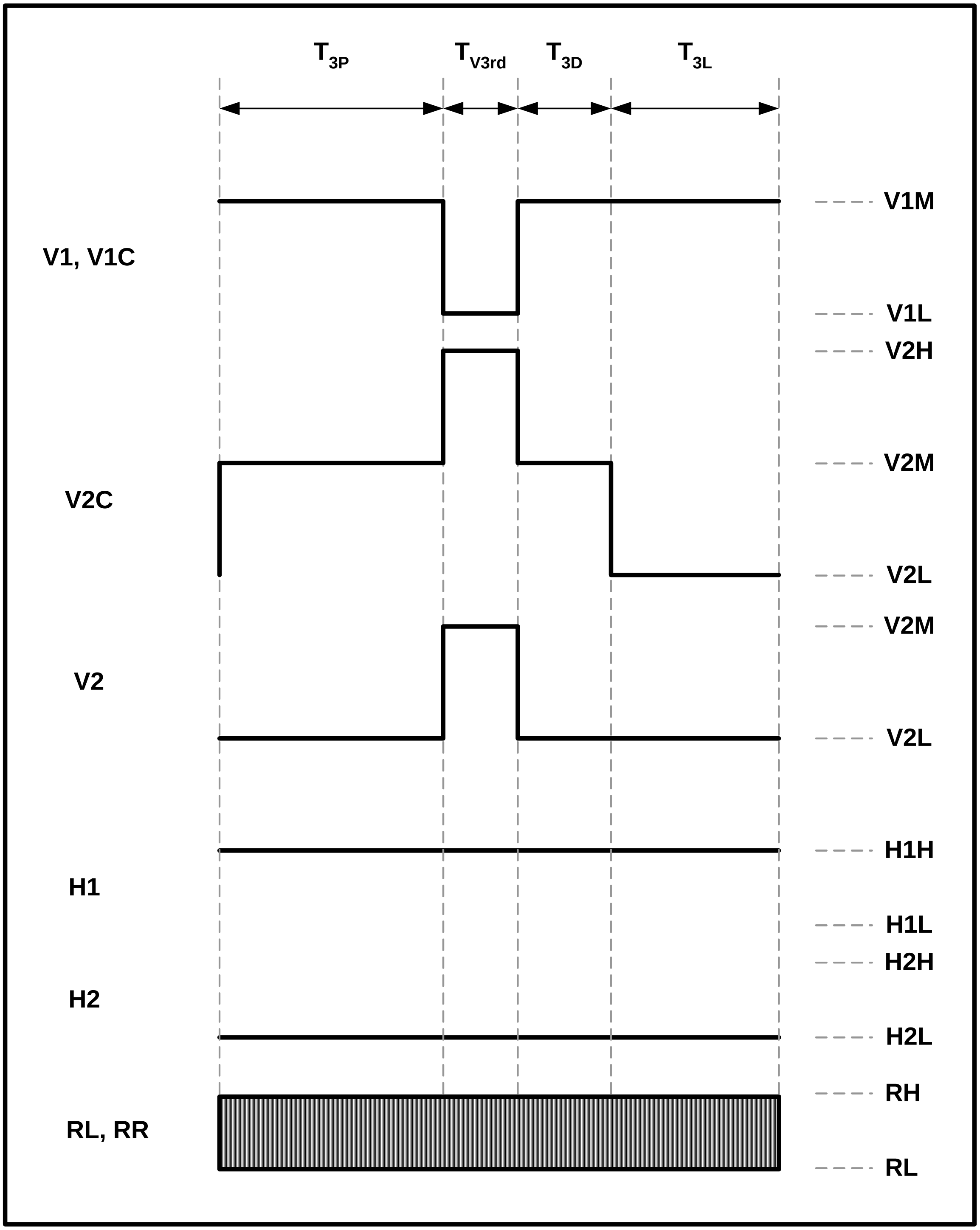


Figure 14: Timing Sequence C

Timing Sequence D

No vertical CCD line transfer, and readout of one horizontal CCD line.

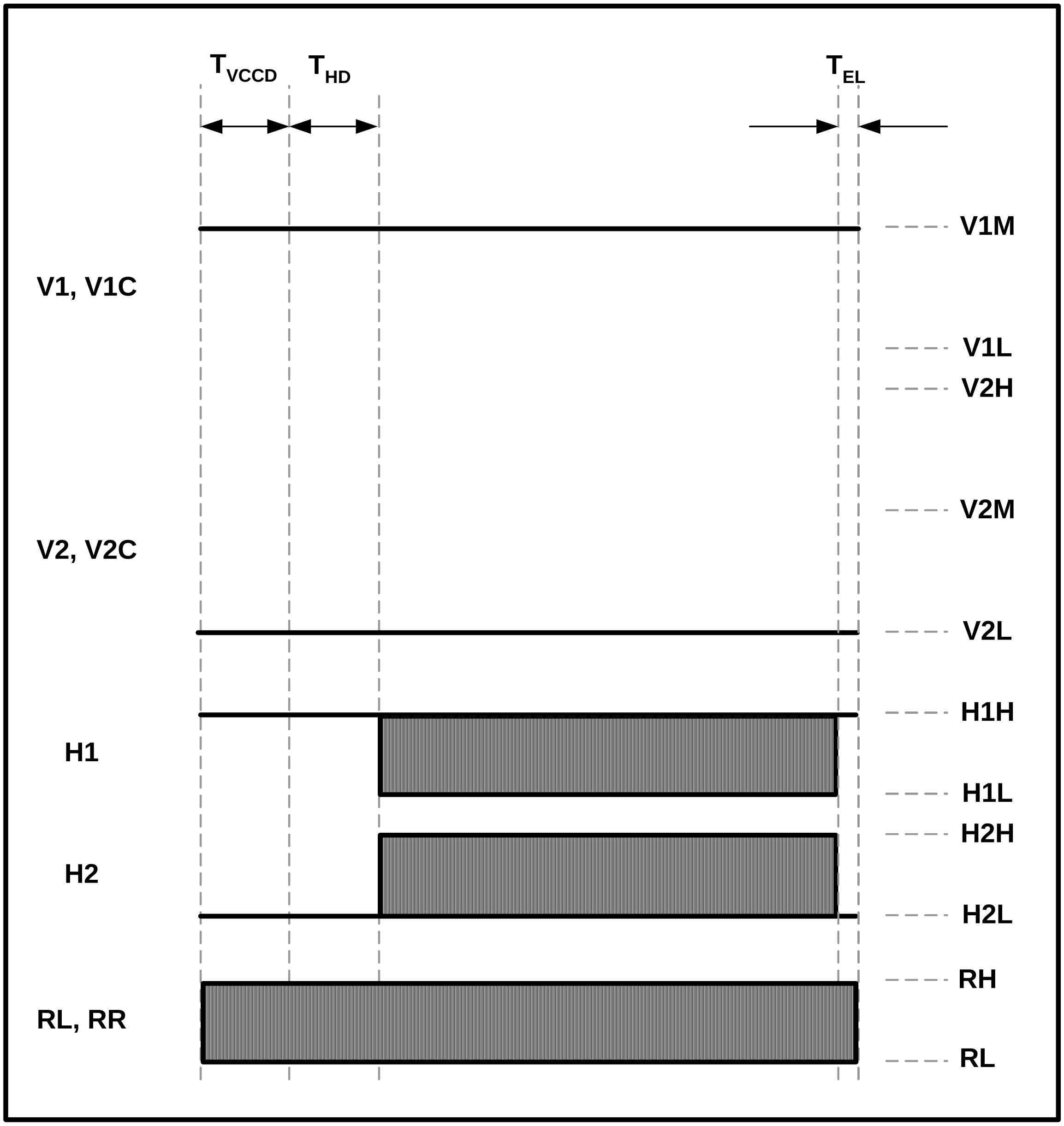
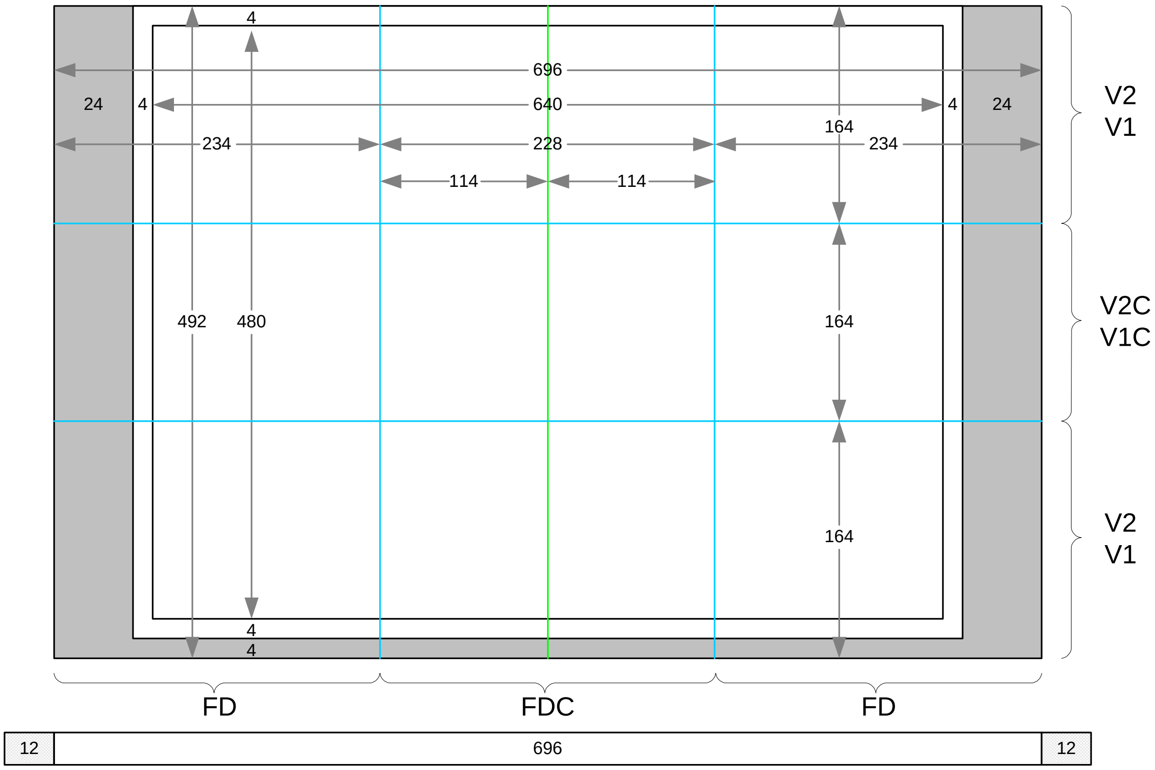


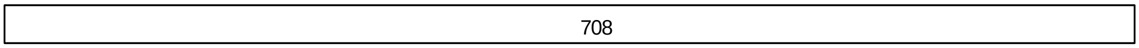
Figure 15: Timing Sequence D

TIMING MODES

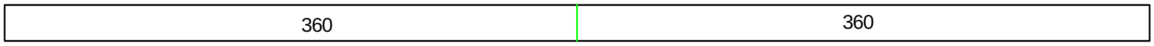
Sensor Architecture



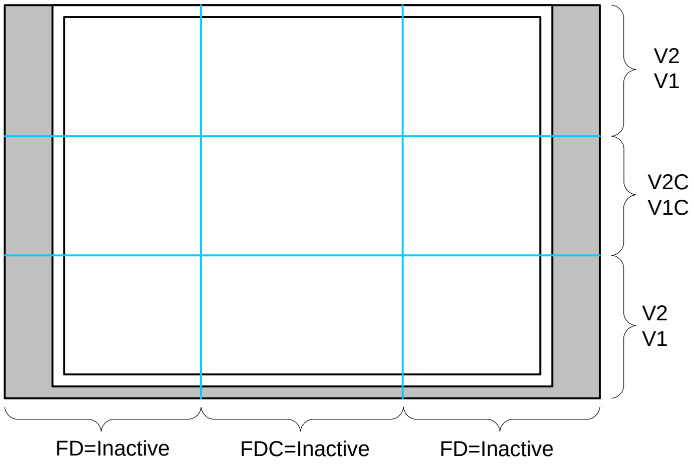
When the sensor is operated in single output mode using the left output, the horizontal CCD is 708 pixels long. This assumes no horizontal over clocking is done.

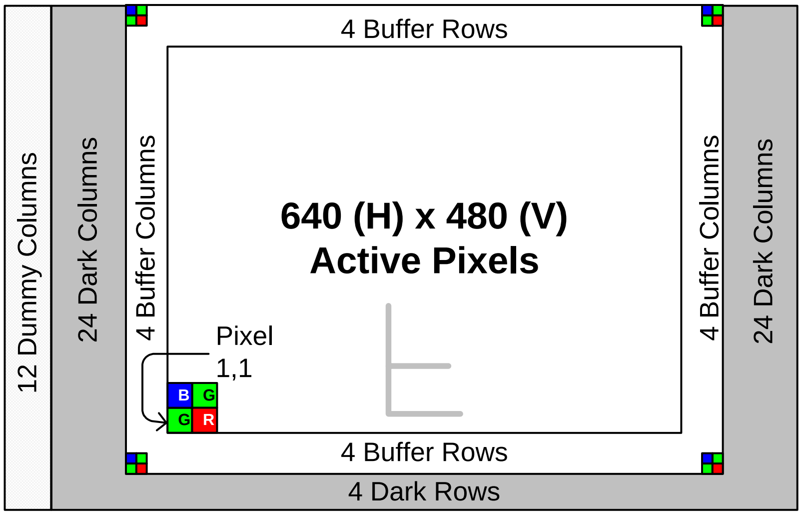


When the sensor is operated in dual output mode, the horizontal CCD is dived into left and right registers. Each half of the register is 360 pixels long. This assumes no horizontal over clocking is done.



One Output Full Field



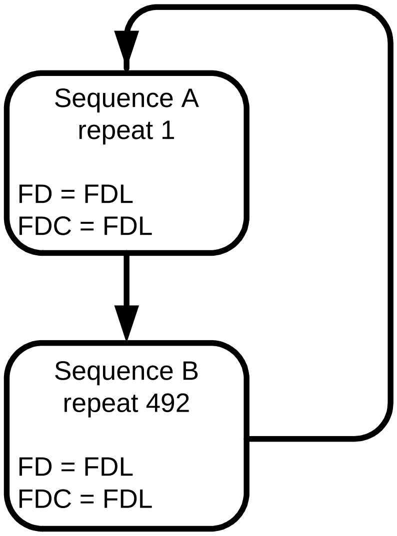


708 HCCD clock cycles per line
492 VCCD clock cycles

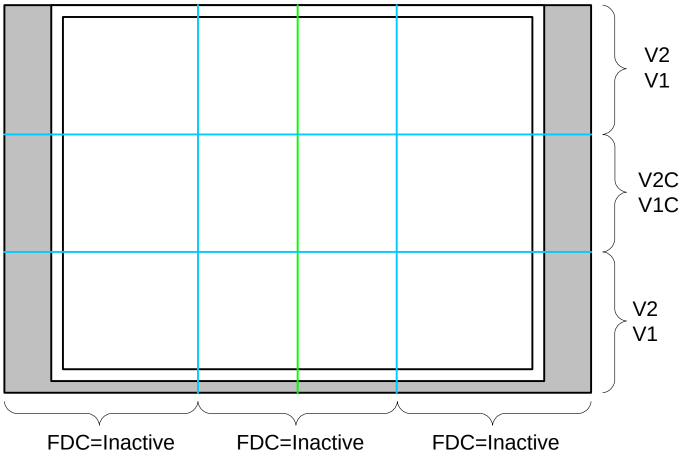
VCCD overclocking: allowed
HCCD overclocking: allowed

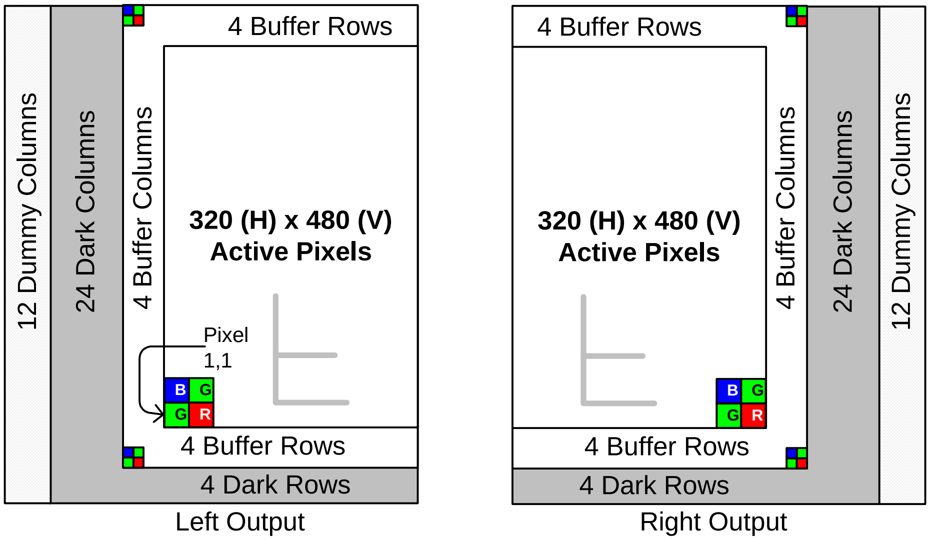
H1 timing: connect to H1S, H1BL, H2BR
H2 timing: connect to H2S, H2BL, H1BR

FDH = Active
FDL = Inactive



Two Outputs Full Field



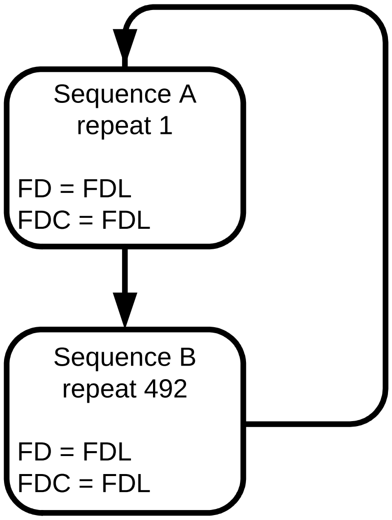


360 HCCD clock cycles per line
492 VCCD clock cycles

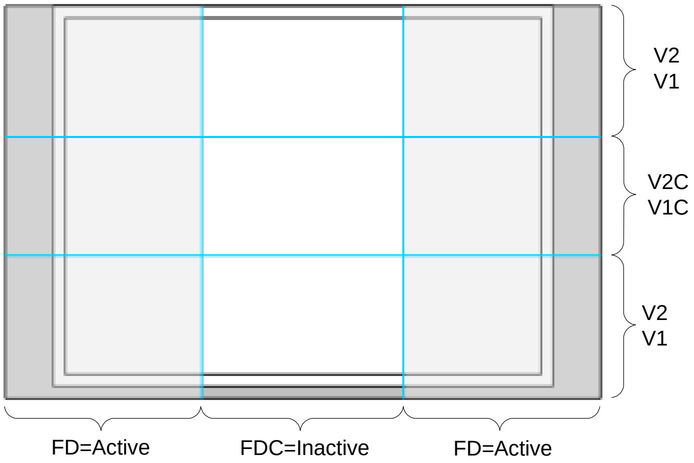
VCCD overclocking: allowed
HCCD overclocking: allowed

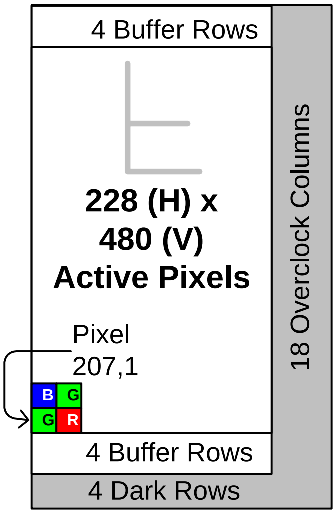
H1 timing: connect to H1S, H1BL, H1BR
H2 timing: connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive



One Output Center Columns



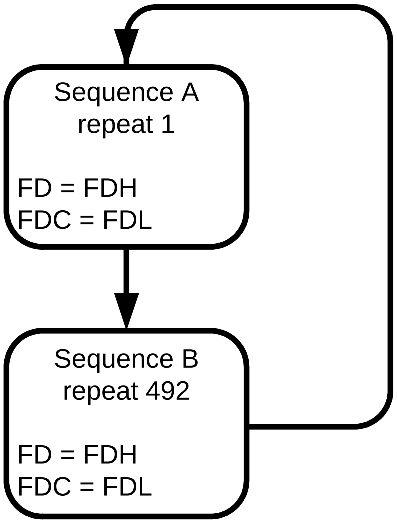


246 HCCD clock cycles per line
492 VCCD clock cycles

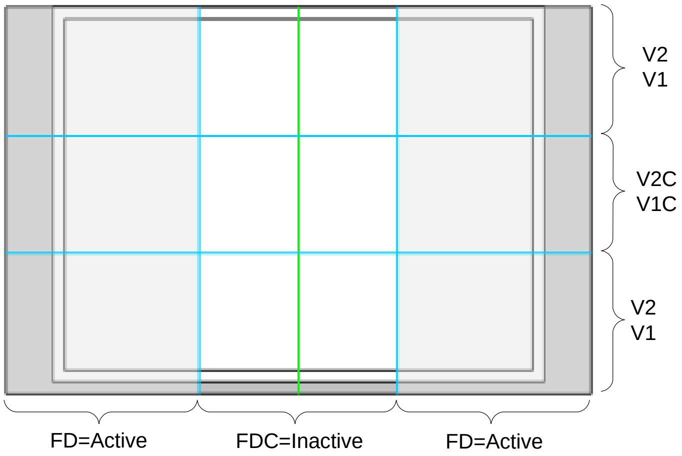
VCCD overclocking: allowed
HCCD overclocking: not allowed

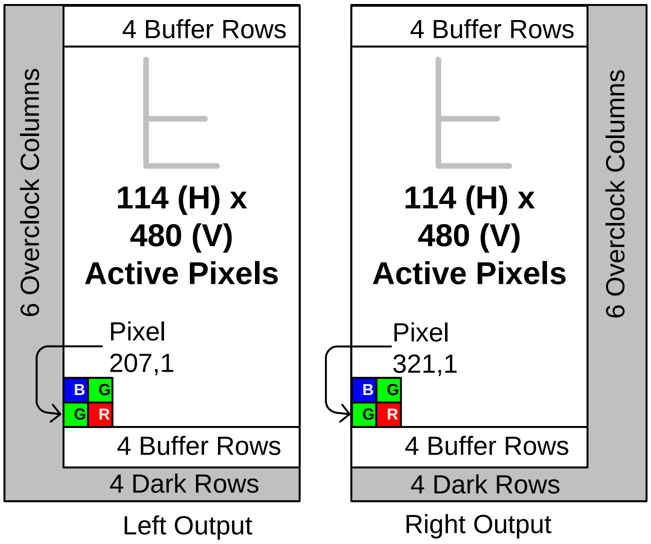
H1 timing: connect to H1S, H1BL, H2BR
H2 timing: connect to H2S, H2BL, H1BR

FDH = Active
FDL = Inactive



Two Outputs Center Columns



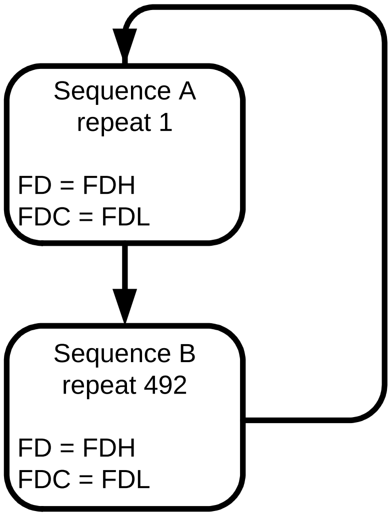


120 HCCD clock cycles per line
492 VCCD clock cycles

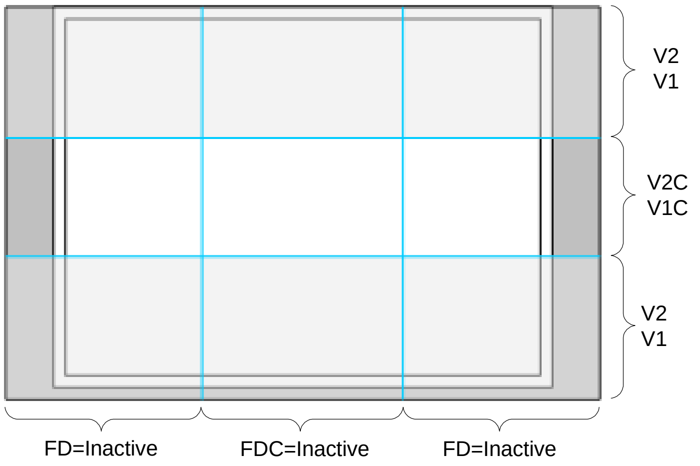
VCCD overclocking: allowed
HCCD overclocking: not allowed

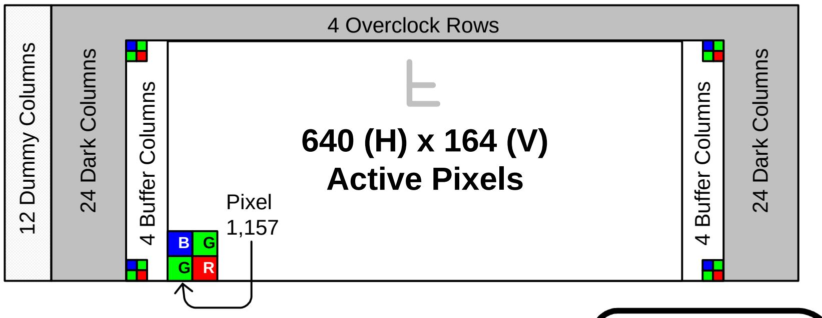
H1 timing: connect to H1S, H1BL, H1BR
H2 timing: connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive



One Output Center Rows



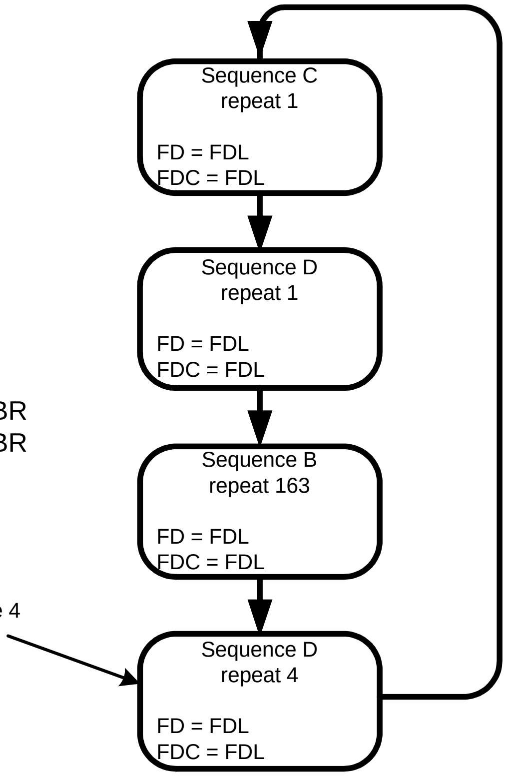


708 HCCD clock cycles per line
163 VCCD clock cycles

VCCD overclocking: not allowed
HCCD overclocking: allowed

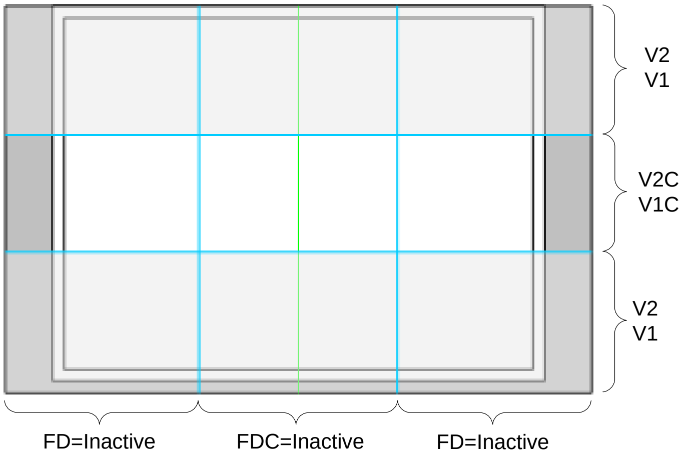
H1 timing: connect to H1S, H1BL, H2BR
H2 timing: connect to H2S, H2BL, H1BR

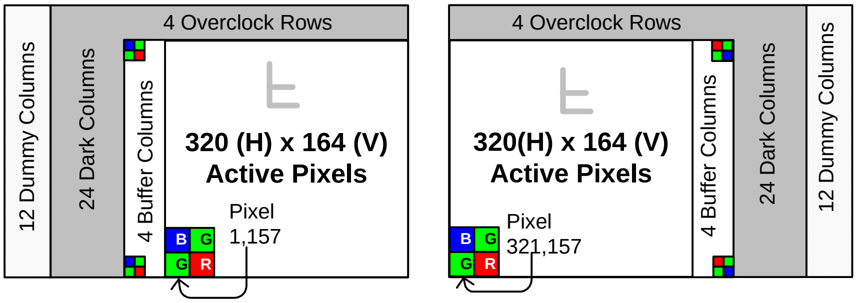
FDH = Active
FDL = Inactive



Omit this step if the 4 overclock rows are not needed

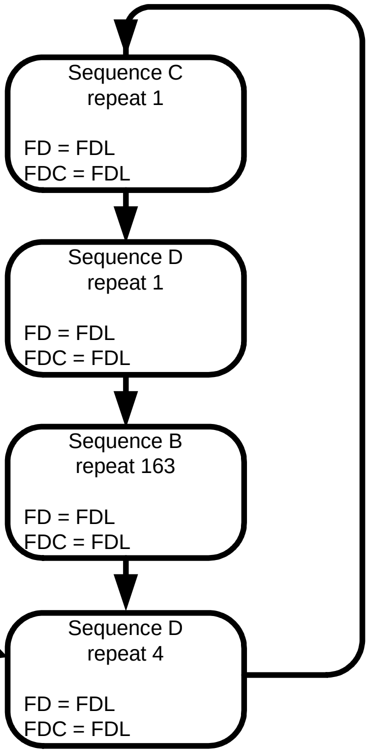
Two Outputs Center Rows





Left Output

Right Output



Omit this step if the 4 overclock rows are not needed

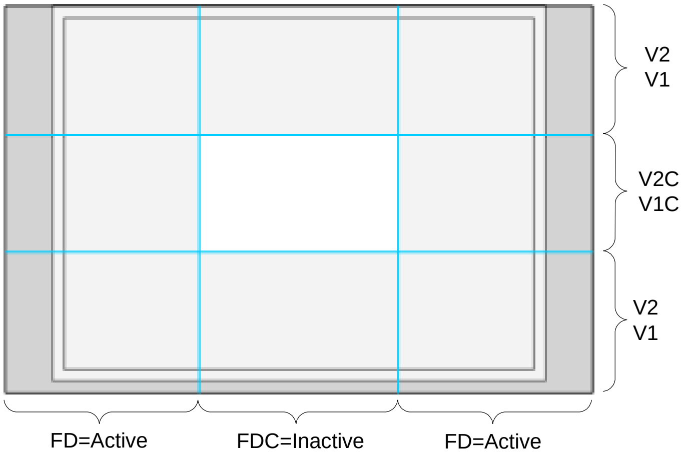
360 HCCD clock cycles per line
163 VCCD clock cycles

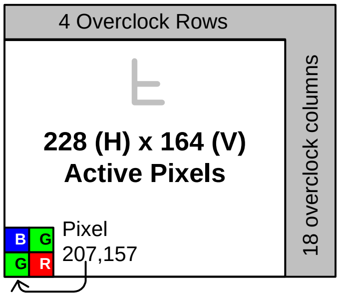
VCCD overclocking: not allowed
HCCD overclocking: allowed

H1 timing: connect to H1S, H1BL, H1BR
H2 timing: connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive

One Output Center Rows and Columns



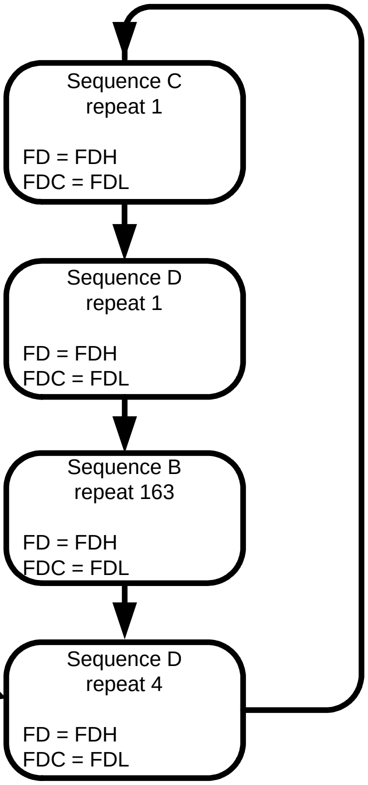


246 HCCD clock cycles per line
163 VCCD clock cycles

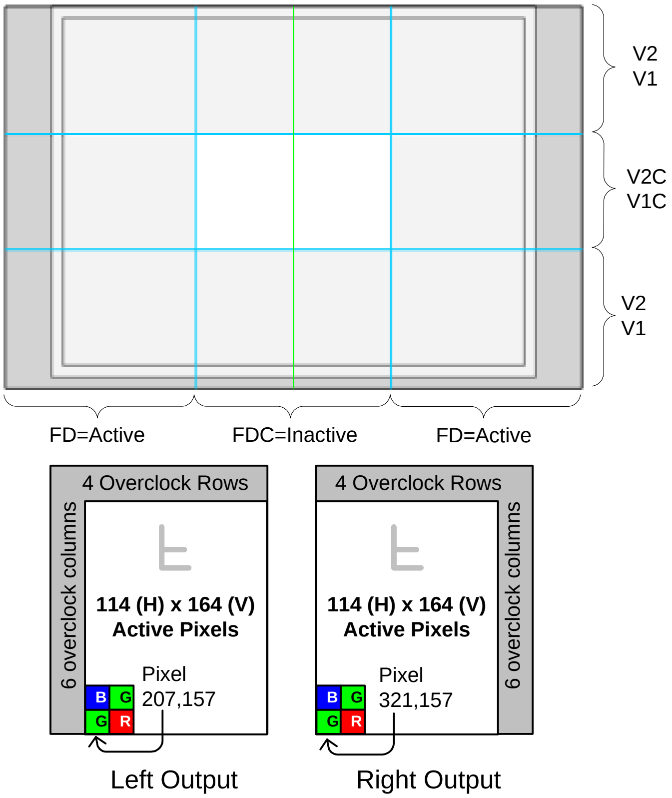
VCCD overclocking: not allowed
HCCD overclocking: not allowed

H1 timing: connect to H1S, H1BL, H2BR
H2 timing: connect to H2S, H2BL, H1BR

FDH = Active
FDL = Inactive



Two Outputs Center Rows and Columns

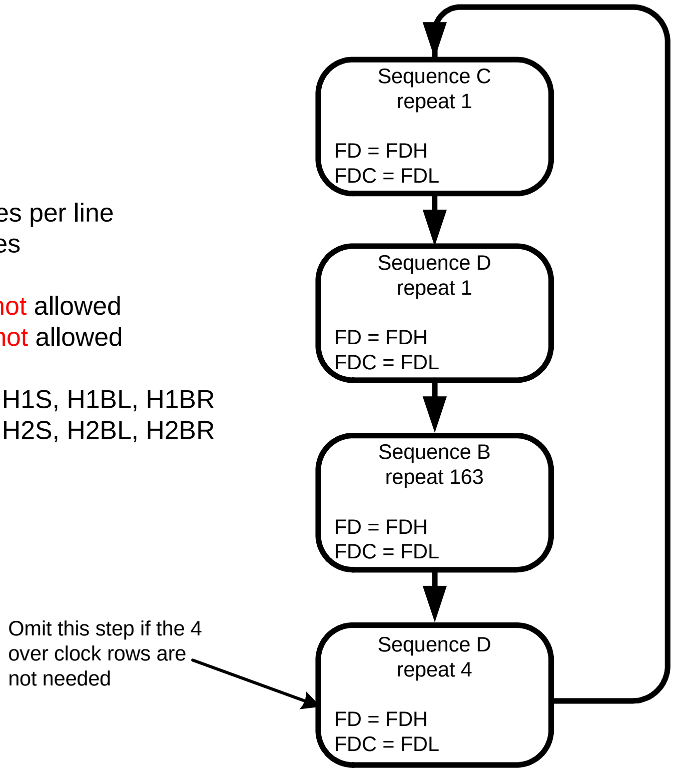


120 HCCD clock cycles per line
163 VCCD clock cycles

VCCD overclocking: not allowed
HCCD overclocking: not allowed

H1 timing: connect to H1S, H1BL, H1BR
H2 timing: connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive



TIMING DETAILS

Pixel Timing

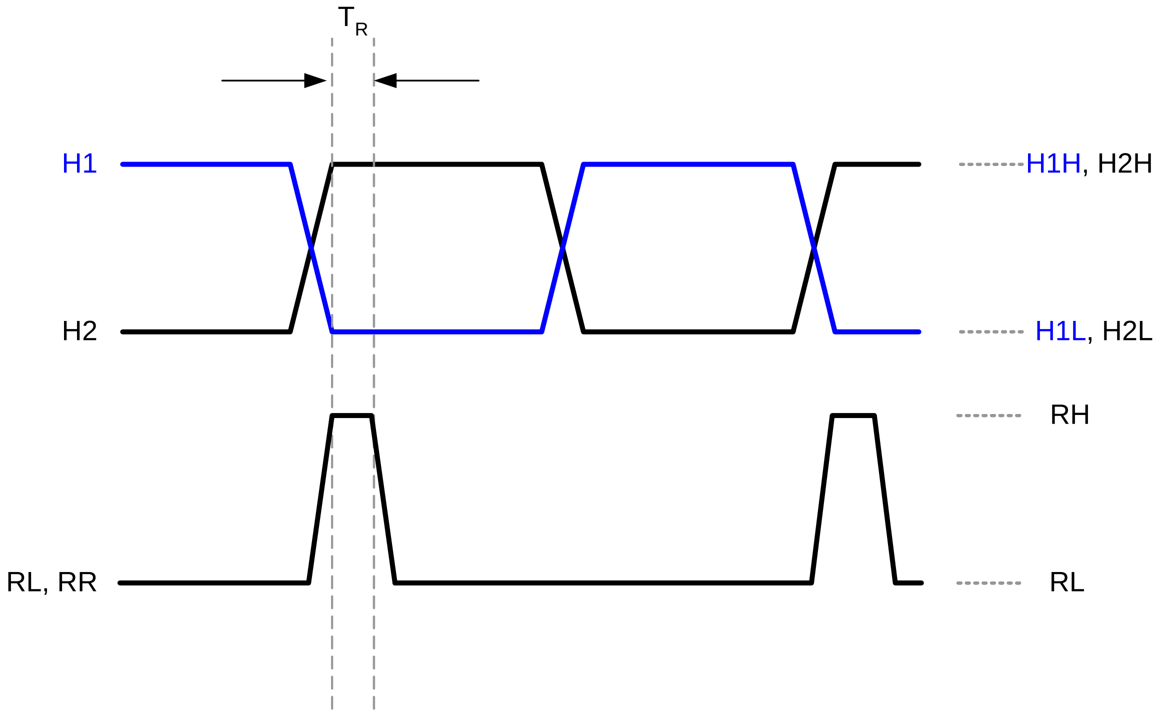


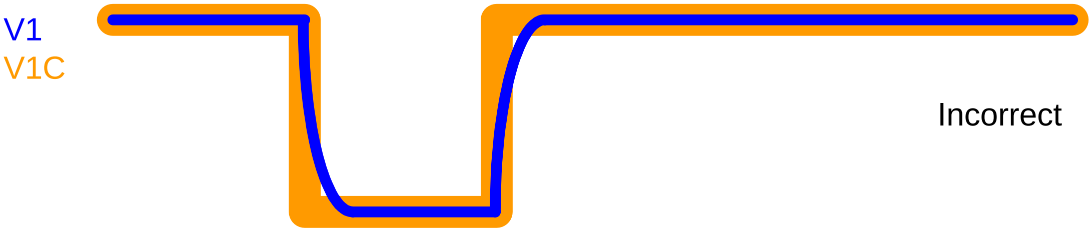
Figure 16: Pixel Timing Detail

Vertical Clock Phase 1 – Line Timing Detail

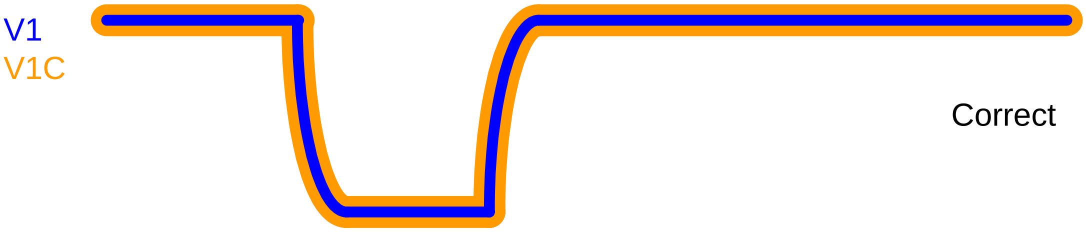
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V1 and V1C pins should be tied together and driven from one clock driver.

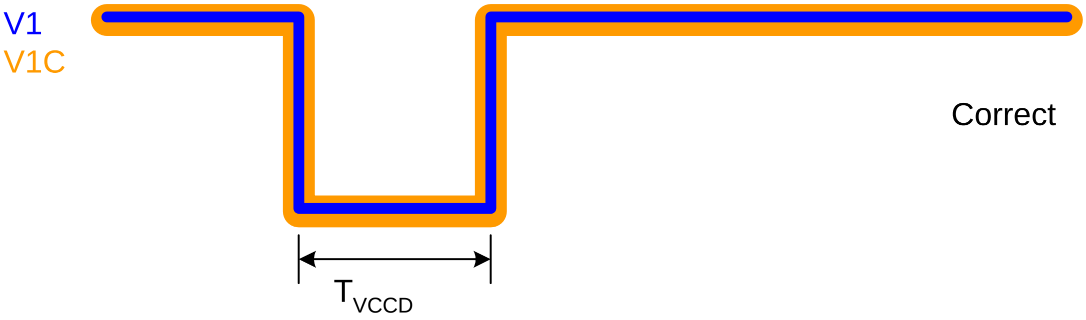
During the line timing, the V1 and V1C rise and fall times need to be identical. Since the V1 capacitance is approximately twice the V1C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V1 and V1C clock waveforms.



The figures below are examples of acceptable V1 and V1C clock waveforms.



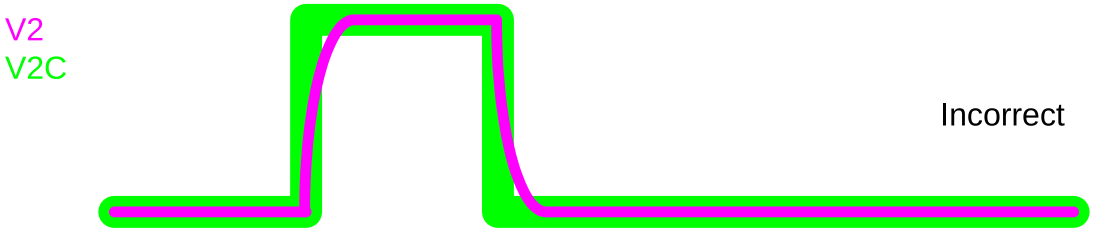


Vertical Clock Phase 2 – Line Timing Detail

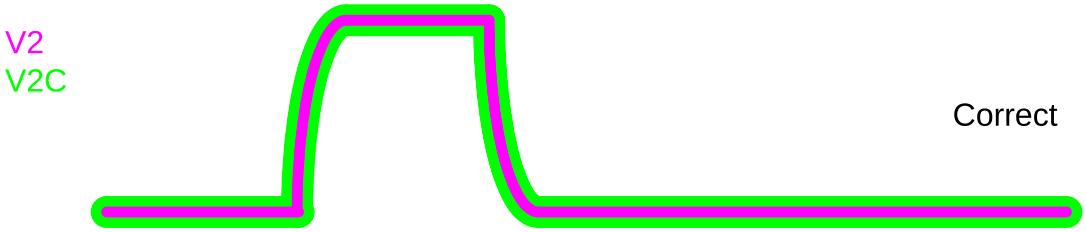
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V2 and V2C pins should be tied together and driven from one clock driver.

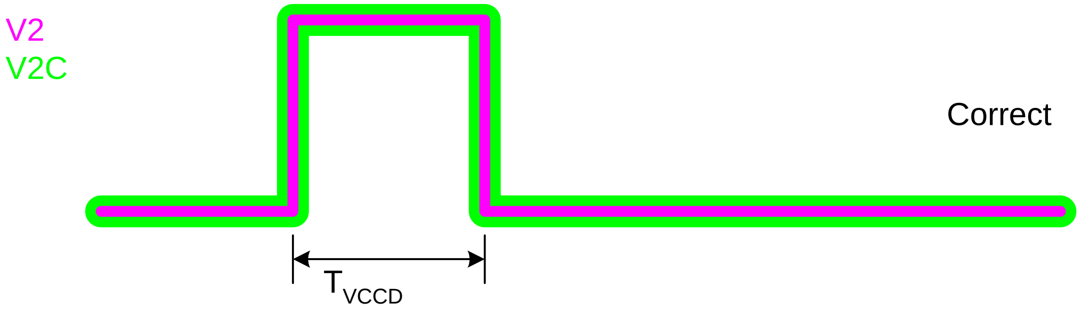
During the line timing, the V2 and V2C rise and fall times need to be identical. Since the V2 capacitance is approximately twice the V2C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V2 and V2C clock waveforms.



The figures below are examples of acceptable V2 and V2C clock waveforms.

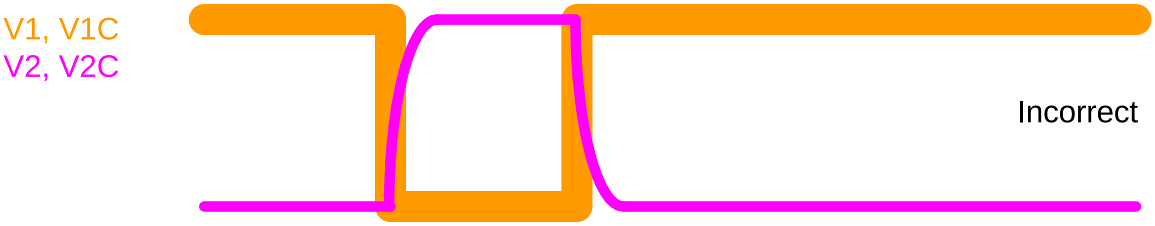




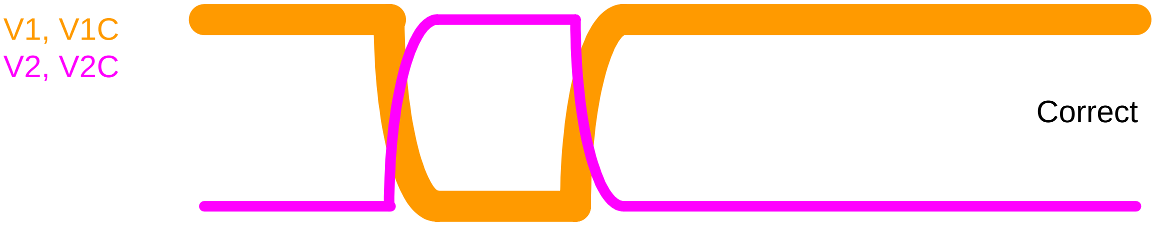
Vertical Clocks Phases 1 and 2 – Line Timing Detail

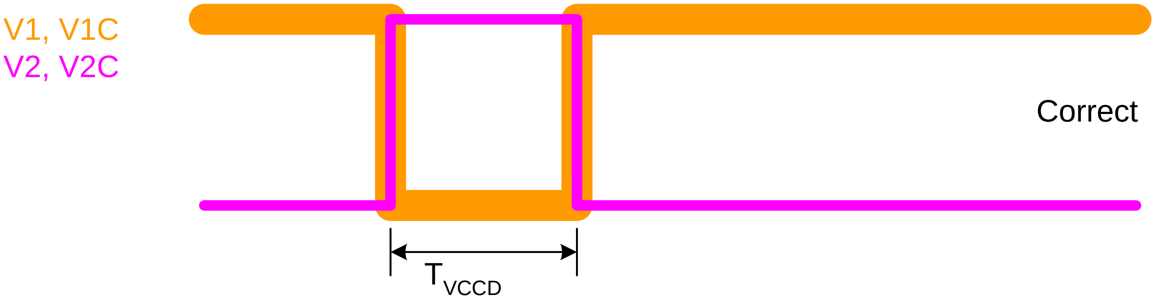
The following line timing detail applies to all modes.

The V1 and V1C clocks must be symmetrical to the V2 and V2C clocks. The figure below is an example of unacceptable V1, V1C, V2 and V2C clock waveforms.



The figures below are of acceptable V1, V1C, V2 and V2C clock waveforms.



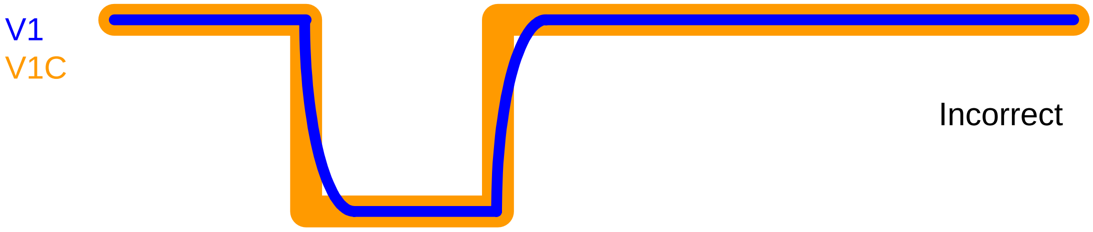


Vertical Clock Phase 1 – Frame Timing Detail

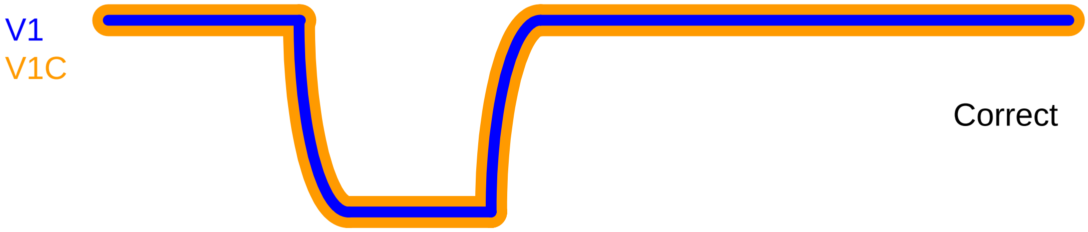
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V1 and V1C pins should be tied together and driven from one clock driver.

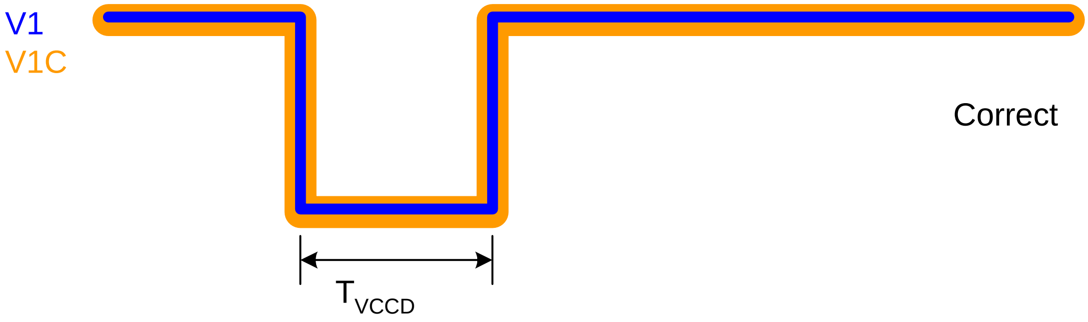
During the frame timing, the V1 and V1C rise and fall times need to be identical. Since the V1 capacitance is approximately twice the V1C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V1 and V1C clock waveforms.



The figures below are examples of acceptable V1 and V1C clock waveforms



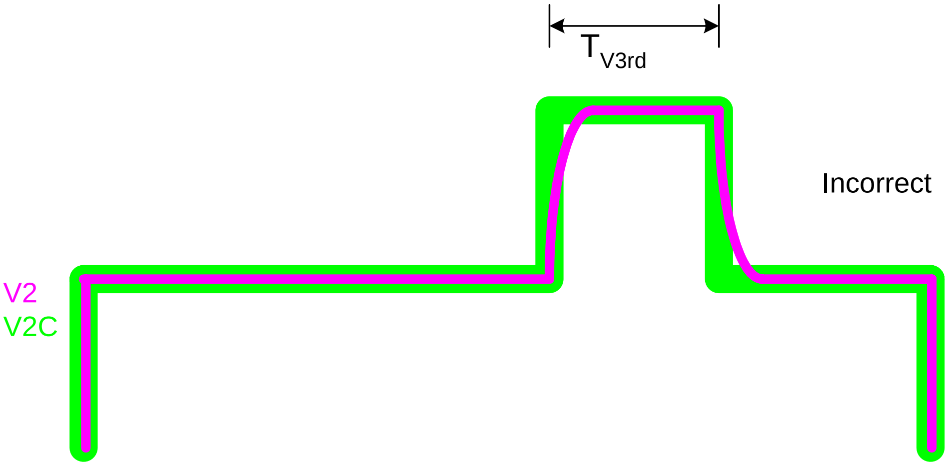


Vertical Clock Phase 2 – Frame Timing Detail

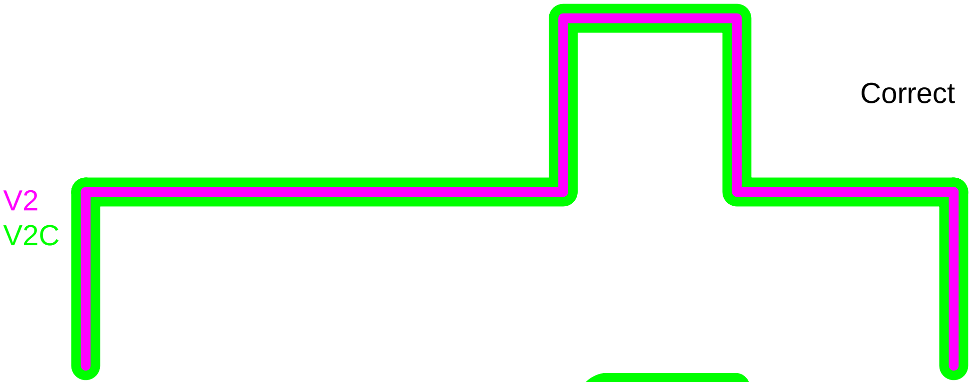
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V2 and V2C pins should be tied together and driven from one clock driver.

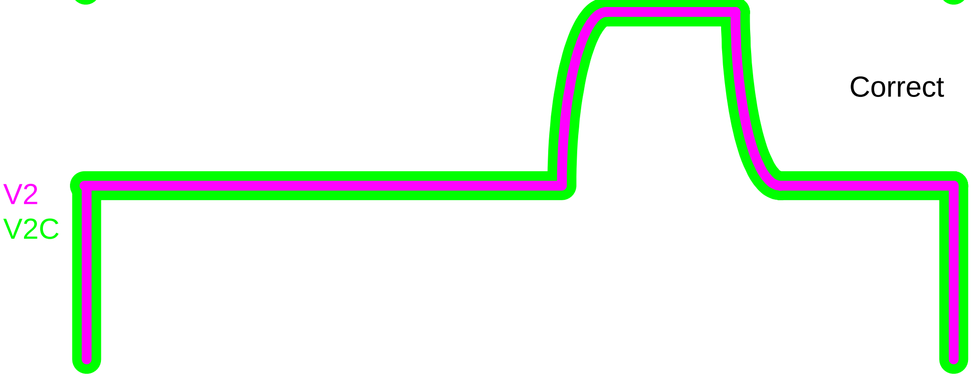
During the frame timing, the V2 and V2C rise and fall times need to be identical. Since the V2 capacitance is approximately twice the V2C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V2 and V2C clock waveforms during the frame timing.



The figures below are examples of acceptable V2 and V2C clock waveforms during the frame timing.



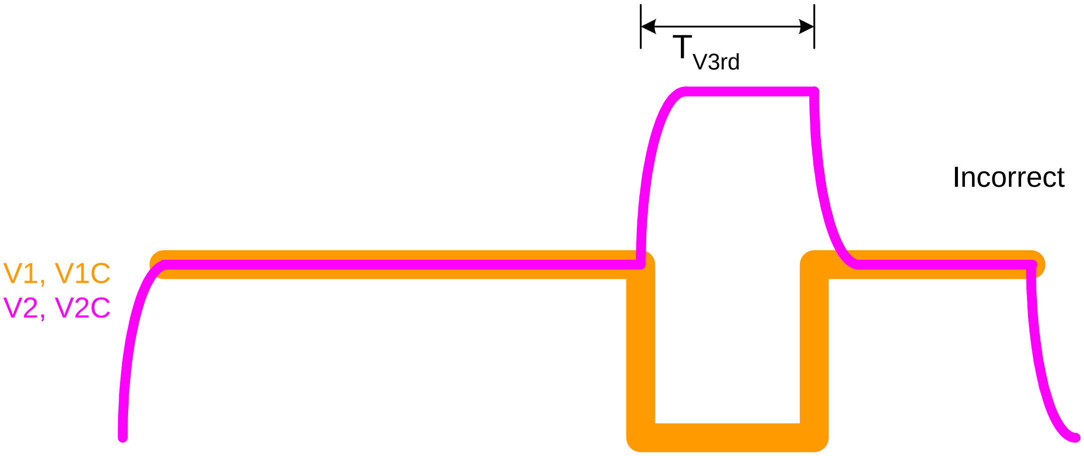


Vertical Clocks Phases 1 and 2 – Frame Timing Detail

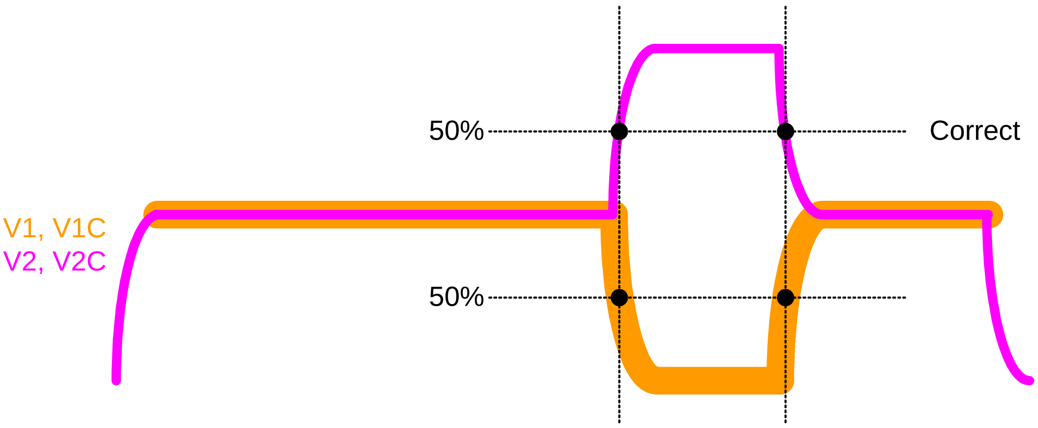
The following frame timing detail applies to all modes.

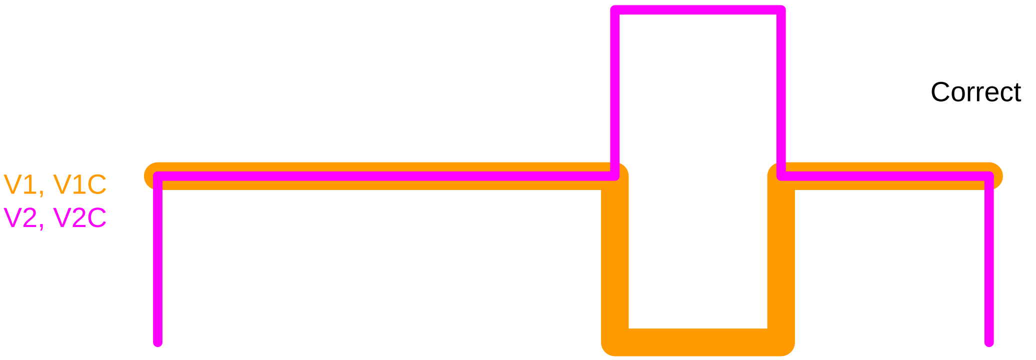
The V1 and V1C clocks must be symmetrical to the V2 and V2C clocks. Also, during the T_{v3rd} timing, the V1 and V2 waveform edges should be aligned to occur at the same time.

The figure below is an example of unacceptable V1, V1C, V2 and V2C clock waveforms.



The figures below are of acceptable V1, V1C, V2 and V2C clock waveforms.





Electronic Shutter Timing

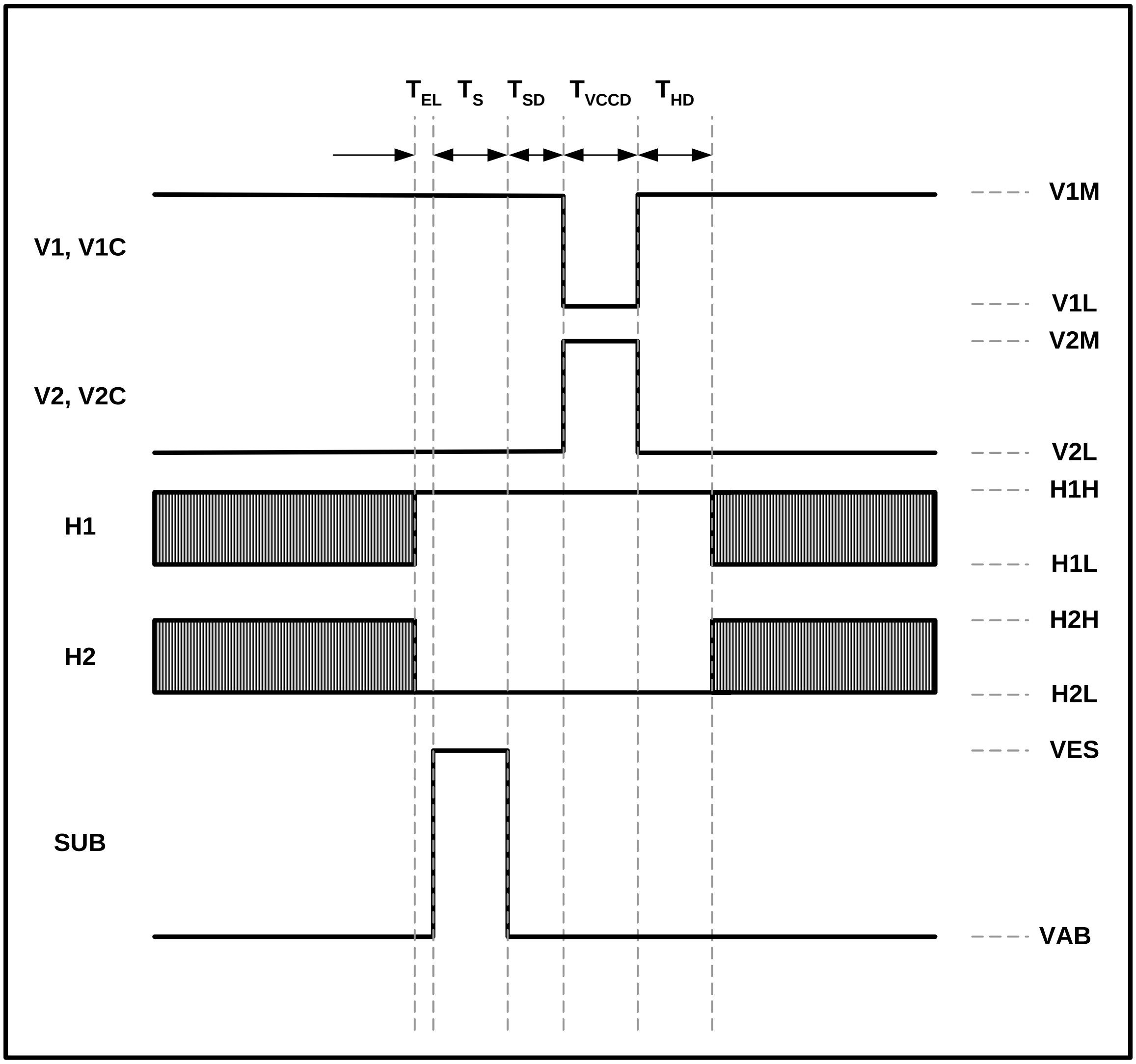


Figure 17: Electronic Shutter Timing

Electronic Shutter – Integration Time Definition

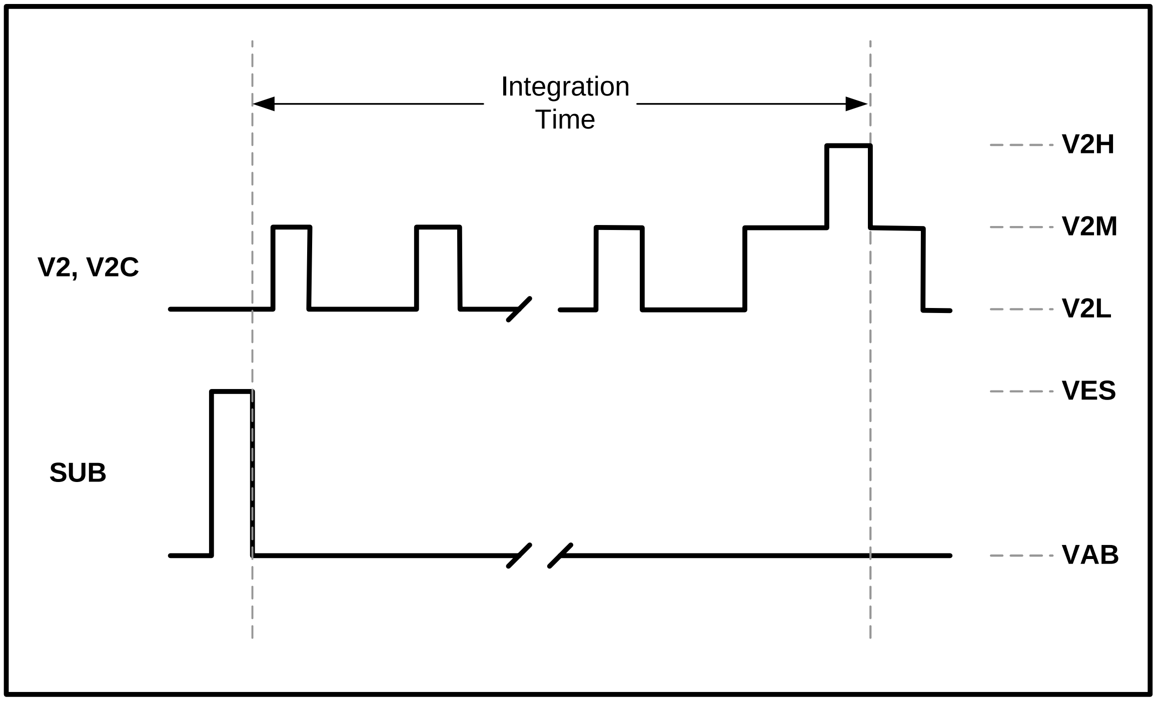


Figure 18: Integration Time Definition

Fast Line Dump Timing

The figure below shows an example of dumping three lines for all rows.

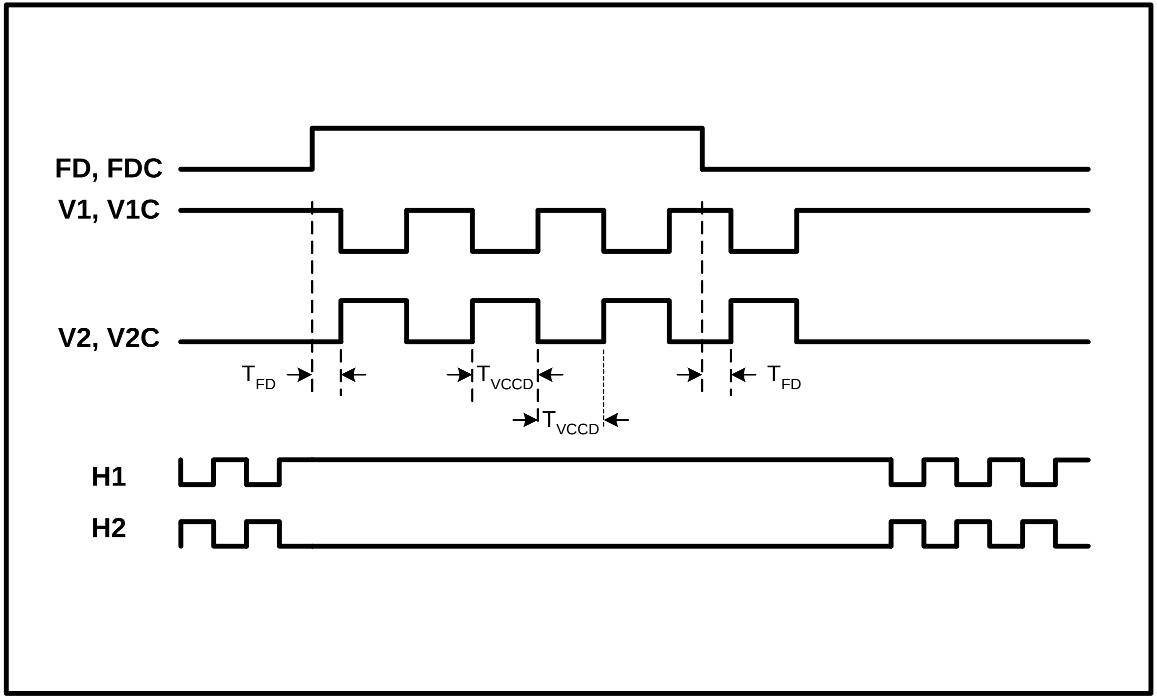
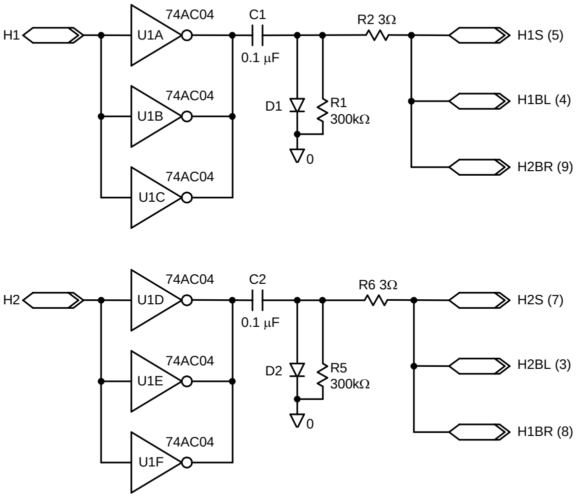


Figure 19: Fast Line Dump Timing

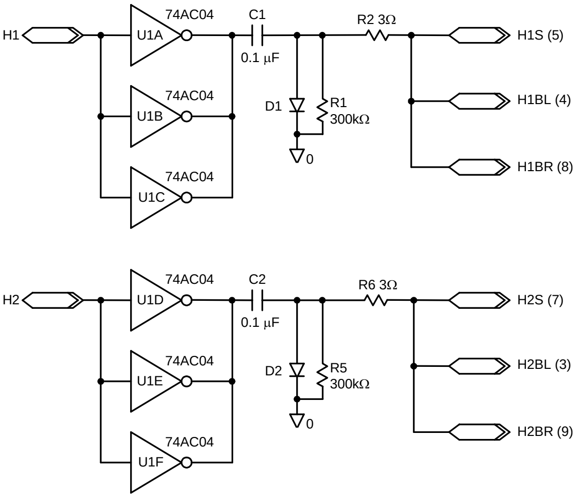
EXAMPLE HCCD CLOCK DRIVER

The HCCD clock inputs should be driven by buffers capable of driving a capacitance of 40pF and having a full voltage swing of at least 4.7 Volts. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a 0.0 to −5.0V clock. This clock level can be obtained by capacitive coupling and a diode to clamp the high level to ground. Resistors R2 and R6 are used to dampen the signal to prevent overshoots. The values of resistors R2 and R6 shown in the schematics below are only suggestions. The actual value required should be selected for each camera design.

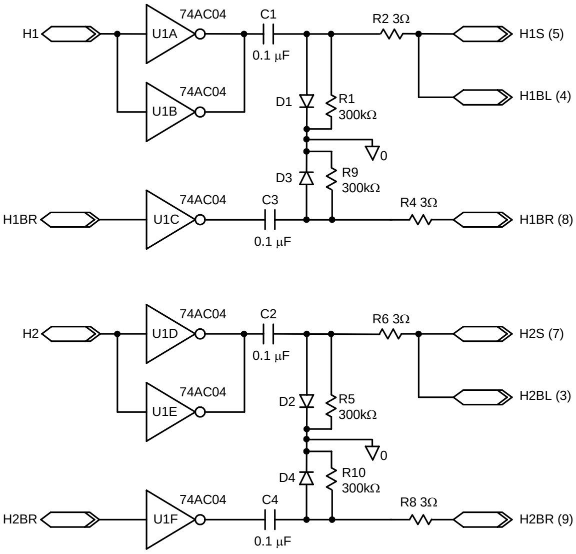
Single Output Only



Dual Output Only



Selectable Single or Dual Output



The inputs to the above circuits, H1 and H2, are 5V logic from the timing generator (a programmable gate array for example). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the H1BR and H2BR timing. For single output mode program the timing such that H1BR=H2 and H2BR=H1. For dual output mode program the timing such that H1BR=H1 and H2BR=H2.

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	80	°C	1
Humidity	RH	5	90	%	2

Notes:

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25°C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices"
4. Each sensor is shipped with a protective tape on the cover glass. The tape should be removed upon usage of the sensor. Care should be used when removing the tape to prevent ESD damage. The tape should be removed when the sensor is in the shipping container or when the sensor is in a camera.

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL DRAWINGS

PACKAGE

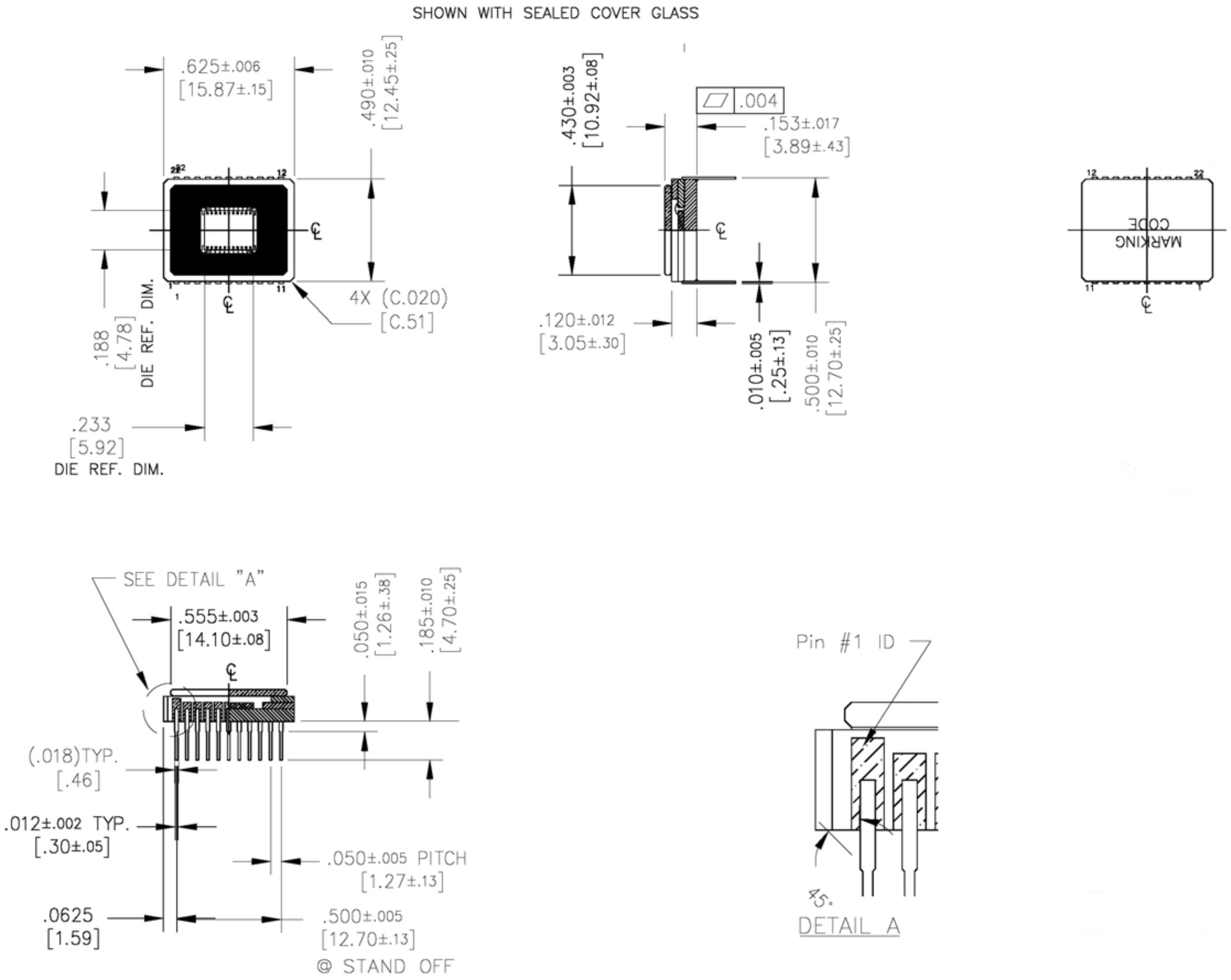


Figure 20: Package Drawing

Notes:

1. Units: IN [mm]
2. See Available Part Configurations in Ordering Section for a description of the marking code.
3. Lid shall not extend beyond ceramic edge.
4. Light shield shown for reference only. Quartz version is smaller.

DIE TO PACKAGE ALIGNMENT

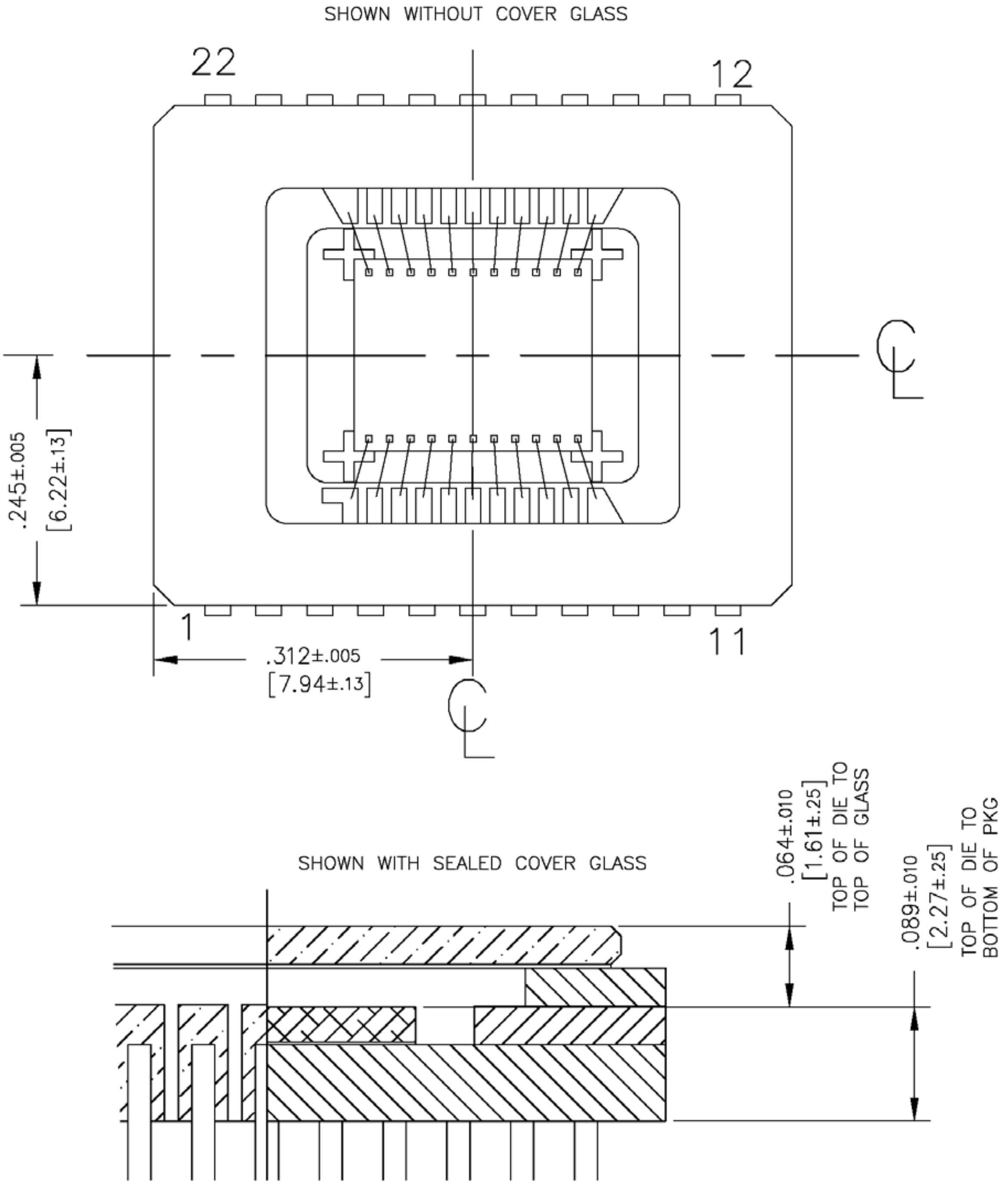


Figure 21: Die to Package Alignment

Notes:

1. Units: IN [mm]
2. Center of image area is offset from center of package by (0.00, 0.00)IN nominal.
3. Die is aligned within ±1 degree of any package cavity edge.

GLASS

Clear Cover Glass

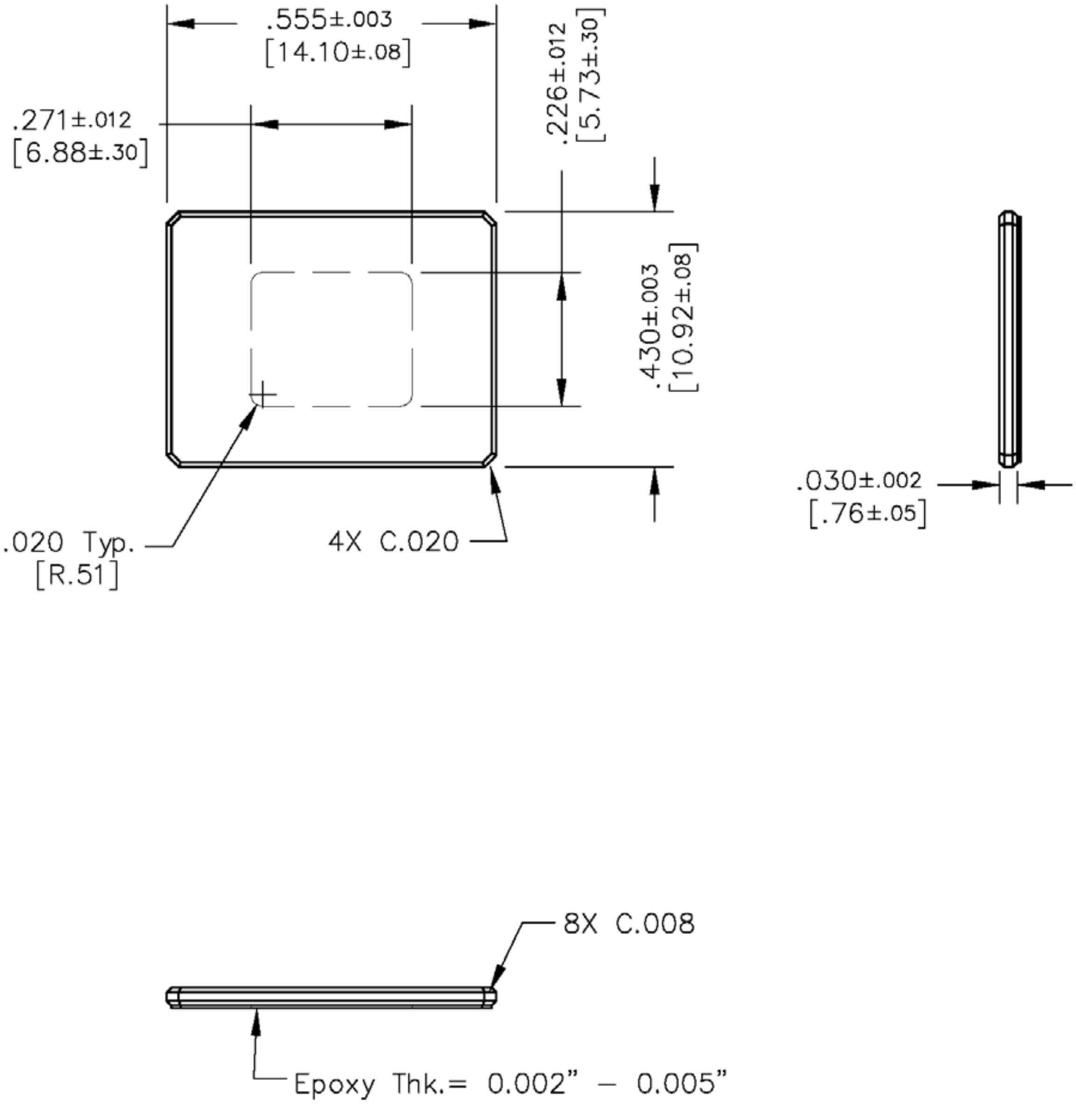


Figure 22: Glass Drawing

Notes:

1. Substrate: Schott D-263
2. Units: Inch [mm]
3. Top and Bottom edge chamfers = 0.008 [0.20]
4. Corner chamfers = 0.020 [0.50]
5. Dust, scratch, dig specification: 10 microns max.

Quartz Cover Glass

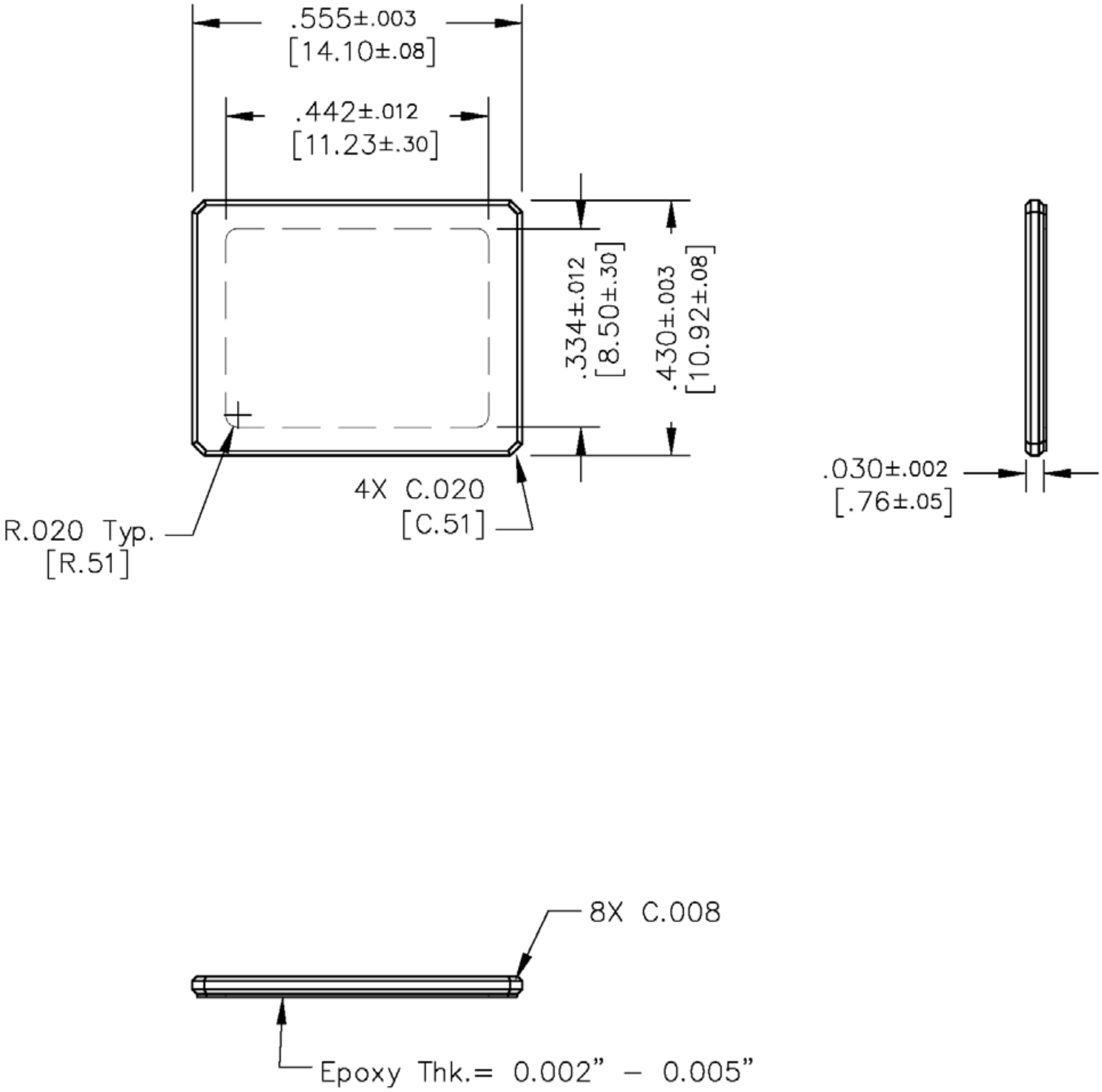


Figure 23: Quartz Cover Glass

Notes:

1. Substrate: SK1300
2. Units: Inch [mm]
3. Top and Bottom edge chamfers = 0.008 [0.20]
4. Corner chamfers = 0.020 [0.50]
5. Dust, scratch, dig specification: 10 microns max.

GLASS TRANSMISSION

Clear Cover Glass

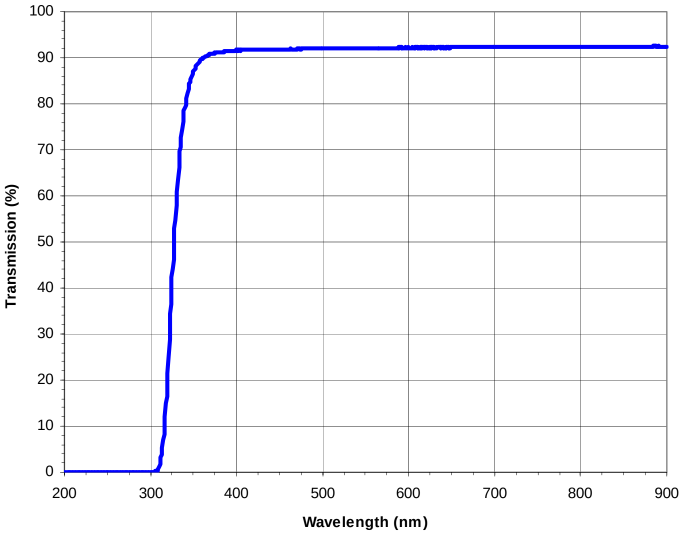


Figure 24: Clear Cover Glass Transmission

Quartz Cover Glass

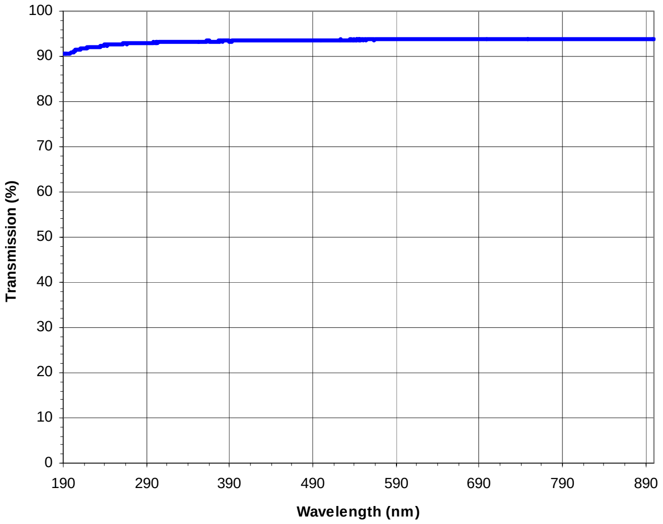


Figure 25: Quartz Cover Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note "Quality and Reliability" (MTD/PS-0292).

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note "Quality and Reliability" (MTD/PS-0292).

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	• Initial formal release
1.1	• Page 26 – Removed caution for cover glass protective tape. The use of the protective tape has been discontinued. • Page 48 – Removed note under Cover Glass Care and Cleanliness section that referred to cover glass protective tape.
2.0	• Updated format • Pages 13 and 18 – Included defect definitions. • Pages 48, 49, 50 and 51 – Updated package and cover glass drawings. • Page 54 – Updated ordering information section.
3.0	• Updated Summary Specification page • Moved and updated Ordering Information page • Updated Monochrome with Microlens Quantum Efficiency graph • Clarified Figure 7 title • Updated Storage and Handling section • Added cover glass protective tape note to Cover Glass Care and Cleanliness Section. Tape use was never discontinued as noted in revision 1.1 change • Improved legibility of package and cover glass drawings • Updated Quality Assurance and Reliability section